

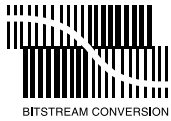


# UDA1384

Multichannel audio coder-decoder

Rev. 02 — 17 January 2005

Product data sheet



## 1. General description

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The UDA1384 is a single-chip consisting of 4 plus 1 Analog-to-Digital Converters (ADC) and 6 Digital-to-Analog Converters (DAC) with signal processing features employing bitstream conversion techniques. The multichannel configuration makes the device eminently suitable for use in digital audio equipment which incorporates surround feature.

The UDA1384 supports conventional 2 channels per line data transfer conformable to the I<sup>2</sup>S-bus format with word lengths of up to 24 bits, the MSB-justified format with word lengths of up to 24 bits and the LSB-justified format with word lengths of 16 bits, 20 bits and 24 bits, as well as 4 channels to 6 channels per line transfer mode. The device also supports a combination of the MSB-justified output format and the LSB-justified input format. The UDA1384 has special sound processing features in the Direct Stream Digital (DSD) playback mode, de-emphasis, volume and mute which can be controlled via the L3-bus or I<sup>2</sup>C-bus interface.

## 2. Features

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### 2.1 General

- 2.7 V to 3.6 V power supply
- 5 V tolerant digital inputs
- 24-bit data path
- Selectable control: via L3-bus or I<sup>2</sup>C-bus microcontroller interface
- Supports sample frequency ranges for:
  - ◆ Audio ADC:  $f_s = 16 \text{ kHz to } 100 \text{ kHz}$
  - ◆ Voice ADC:  $f_s = 7 \text{ kHz to } 50 \text{ kHz}$
  - ◆ Audio DAC:  $f_s = 16 \text{ kHz to } 200 \text{ kHz}$
- Separate power control for ADC and DAC
- ADC plus integrated high-pass filter to cancel DC offset
- Integrated digital filter plus DAC
- Slave mode only applications
- Easy application

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## 2.2 Multiple format data interface

- Audio interface supports standard I<sup>2</sup>S-bus, MSB-justified, LSB-justified and two multichannel formats
- Voice interface supports I<sup>2</sup>S-bus and mono channel formats

## 2.3 Digital sound processing

- Control via L3-bus or I<sup>2</sup>C-bus:
  - ◆ Channel independent digital logarithmic volume
  - ◆ Digital de-emphasis for  $f_s = 32$  kHz, 44.1 kHz, 48 kHz or 96 kHz
  - ◆ Soft or quick mute
  - ◆ Output signal polarity control

## 2.4 Advanced audio configuration

- Inputs:
  - ◆ 4 single-ended audio inputs (2 × stereo) with programmable gain amplifiers
  - ◆ 1 single-ended voice input
- Outputs:
  - ◆ 6 differential audio outputs (3 × stereo)
- DSD mode to support stereo DSD playback
- High linearity, wide dynamic range and low distortion
- DAC digital filter with selectable sharp or soft roll-off

## 3. Applications

- Excellently suitable for multichannel home audio-video application

## 4. Quick reference data

**Table 1: Quick reference data**

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3$  V;  $T_{amb} = 25$  °C;  $R_L = 22$  k $\Omega$ ; all voltages referenced to ground (pins  $V_{SS}$ ); unless otherwise specified.

| Symbol          | Parameter                 | Conditions  | Min | Typ | Max | Unit |
|-----------------|---------------------------|---|-----|-----|-----|------|
| <b>Supplies</b> |                           |   |     |     |     |      |
| $V_{DDA(AD)}$   | ADC analog supply voltage |   | 2.7 | 3.3 | 3.6 | V    |
| $V_{DDA(DA)}$   | DAC analog supply voltage |   | 2.7 | 3.3 | 3.6 | V    |
| $V_{DDD}$       | digital supply voltage    |   | 2.7 | 3.3 | 3.6 | V    |
| $I_{DDA(AD)}$   | ADC analog supply current | $f_{ADC} = 48$ kHz                                    | -   | 30  | -   | mA   |
| $I_{DDA(DA)}$   | DAC analog supply current | $f_{DAC} = 48$ kHz                                    | -   | 20  | -   | mA   |
| $I_{DDD}$       | digital supply current    | $f_{ADC} = f_{DAC} = 48$ kHz;<br>$f_{VOICE} = 48$ kHz | -   | 31  | -   | mA   |

**Table 1: Quick reference data ...continued**

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $R_L = 22\text{ k}\Omega$ ; all voltages referenced to ground (pins  $V_{SS}$ ); unless otherwise specified.

| Symbol                                   | Parameter  | Conditions                         | Min         | Typ  | Max  | Unit |
|--|--|------------------------------------|-------------|------|------|------|
| $I_{DDD(pd)}$                            | digital supply current in Power-down mode            | audio and voice<br>ADCs power-down | -           | 18   | -    | mA   |
|  |  | DAC power-down                     | -           | 14   | -    | mA   |
| $T_{amb}$                                | ambient temperature                                  |                                    | -20         | -    | +85  | °C   |
| <b>Audio analog-to-digital converter</b> |  |                                    |             |      |      |      |
| $D_0$                                    | digital output level                                 | at 0 dB setting;<br>900 mV input   | [1][2] -2.5 | -1.2 | -0.7 | dB   |
| (THD+N)/S                                | total harmonic distortion-plus-noise to signal ratio | at -1 dBFS                         | -           | -88  | -82  | dB   |
|  |  | at -60 dBFS;<br>A-weighted         | -           | -37  | -30  | dB   |
| S/N                                      | signal-to-noise ratio                                | code = 0; A-weighted               | 89          | 98   | -    | dB   |
| $\alpha_{cs}$                            | channel separation                                   |                                    | -           | 100  | -    | dB   |
| <b>Digital-to-analog converter</b>       |  |                                    |             |      |      |      |
| <b>Differential mode</b>                 |  |                                    |             |      |      |      |
| $V_{o(rms)}$                             | output voltage (RMS value)                           | at 0 dBFS digital input            | 1.9         | 2.0  | 2.1  | V    |
| (THD+N)/S                                | total harmonic distortion-plus-noise to signal ratio | at 0 dBFS                          | -           | -98  | -89  | dB   |
|  |  | at -60 dBFS;<br>A-weighted         | -           | -50  | -45  | dB   |
| S/N                                      | signal-to-noise ratio                                | code = 0; A-weighted               | 100         | 110  | -    | dB   |
| $\alpha_{cs}$                            | channel separation                                   |                                    | -           | 114  | -    | dB   |
| <b>Single-ended mode</b>                 |  |                                    |             |      |      |      |
| $V_{o(rms)}$                             | output voltage (RMS value)                           | at 0 dBFS digital input            | -           | 1.0  | -    | V    |
| (THD+N)/S                                | total harmonic distortion-plus-noise to signal ratio | at 0 dBFS                          | -           | -88  | -    | dB   |
|  |  | at -60 dBFS;<br>A-weighted         | -           | -45  | -    | dB   |
| S/N                                      | signal-to-noise ratio                                | code = 0; A-weighted               | -           | 105  | -    | dB   |
| $\alpha_{cs}$                            | channel separation                                   |                                    | -           | 110  | -    | dB   |

[1] The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.

[2] The input voltage to the ADC scales proportionally with the power supply voltage.

## 5. Ordering information

**Table 2: Ordering information**

| Type number | Package |  | Version  |
|-------------|---------|--|----------|
|             | Name    | Description  |          |
| UDA1384H    | QFP44   | plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm | SOT307-2 |

6. Block diagram

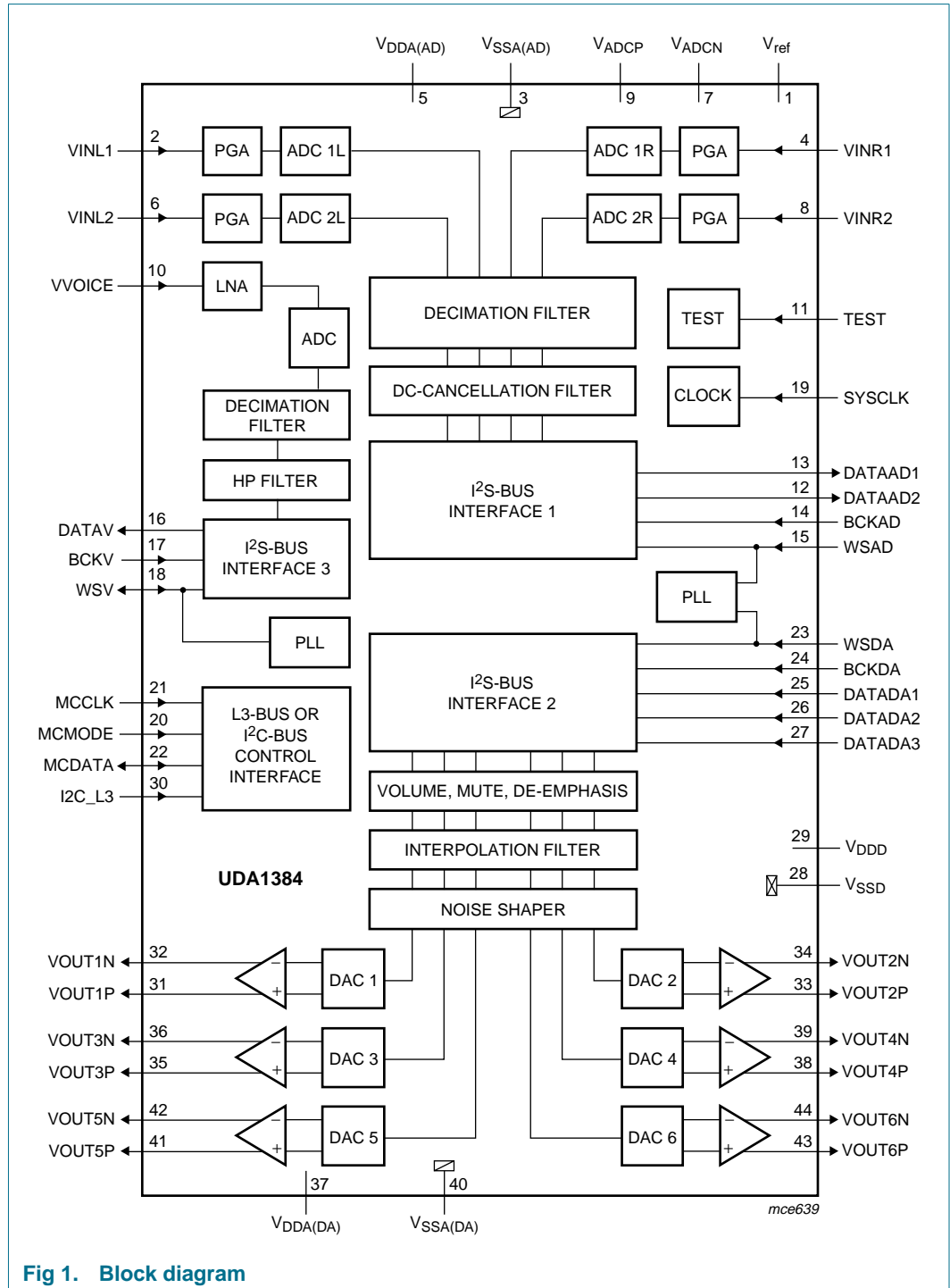


Fig 1. Block diagram

## 7. Pinning information

### 7.1 Pinning

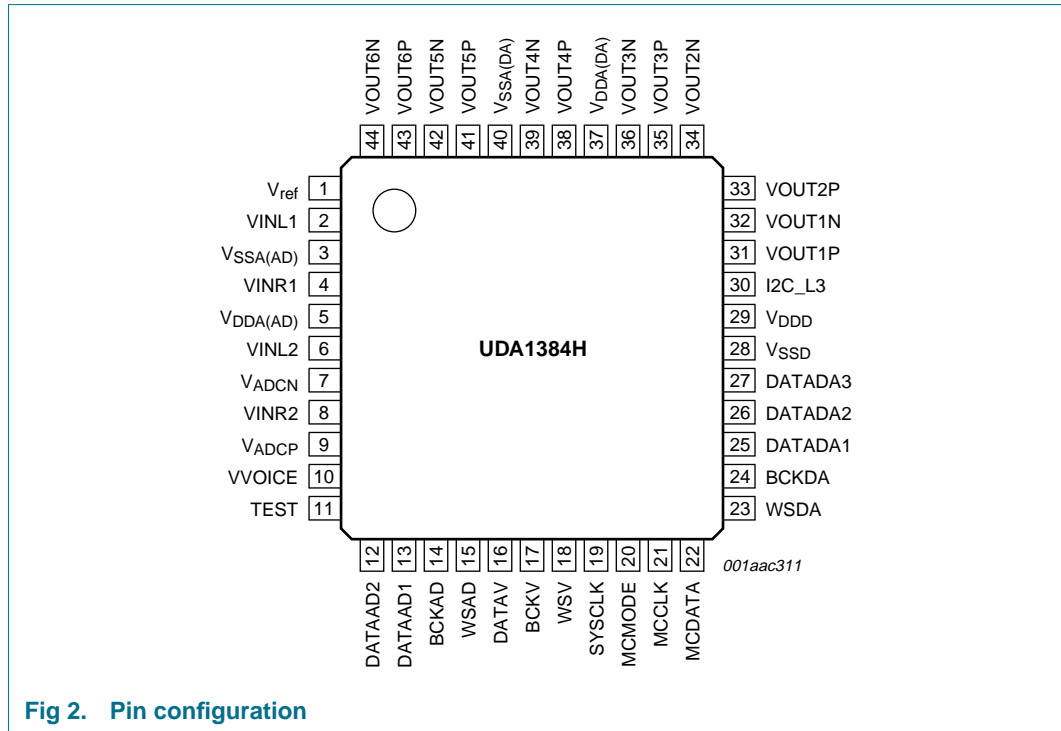


Fig 2. Pin configuration

### 7.2 Pin description

Table 3: Pin description

| Symbol        | Pin | Type | Description  |
|---------------|-----|------|--|
| $V_{ref}$     | 1   | AIO  | ADC reference voltage  |
| VINL1         | 2   | AIO  | ADC 1 input left   |
| $V_{SSA(AD)}$ | 3   | AGND | ADC analog ground  |
| VINR1         | 4   | AIO  | ADC 1 input right  |
| $V_{DDA(AD)}$ | 5   | AS   | ADC analog supply voltage  |
| VINL2         | 6   | AIO  | ADC 2 input left   |
| $V_{ADCN}$    | 7   | AIO  | ADC reference voltage N  |
| VINR2         | 8   | AIO  | ADC 2 input right  |
| $V_{ADCP}$    | 9   | AIO  | ADC reference voltage P  |
| VVOICE        | 10  | AIO  | voice ADC input  |
| TEST          | 11  | DID  | test input; must be connected to digital ground ( $V_{SSD}$ ) in application |
| DATAAD2       | 12  | DO   | ADC 2 data output  |
| DATAAD1       | 13  | DO   | ADC 1 data output  |
| BCKAD         | 14  | DIS  | ADC bit clock input  |
| WSAD          | 15  | DI   | ADC word select input  |

Table 3: Pin description ...continued

| Symbol               | Pin | Type | Description  |
|----------------------|-----|------|--|
| DATAV                | 16  | DO   | voice data output  |
| BCKV                 | 17  | DIS  | voice bit clock input  |
| WSV                  | 18  | DIO  | voice word select input or output  |
| SYSCLK               | 19  | DIS  | system clock input: 256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub> |
| MCMODE               | 20  | DI   | L3-bus L3MODE input or I <sup>2</sup> C-bus DAC mute control input                                 |
| MCCLK                | 21  | DIS  | L3-bus L3CLOCK input or I <sup>2</sup> C-bus SCL input   |
| MCDATA               | 22  | IIC  | L3-bus L3DATA input and output or I <sup>2</sup> C-bus SDA input and output                        |
| WSDA                 | 23  | DI   | DAC word select input  |
| BCKDA                | 24  | DIS  | DAC bit clock input  |
| DATADA1              | 25  | DI   | DAC channel 1 and channel 2 data input   |
| DATADA2              | 26  | DI   | DAC channel 3 and channel 4 data input   |
| DATADA3              | 27  | DI   | DAC channel 5 and channel 6 data input   |
| V <sub>SSD</sub>     | 28  | DGND | digital ground   |
| V <sub>DDD</sub>     | 29  | DS   | digital supply voltage   |
| I2C_L3               | 30  | DI   | selection input for L3-bus or I <sup>2</sup> C-bus control   |
| VOUT1P               | 31  | AIO  | DAC 1 positive output  |
| VOUT1N               | 32  | AIO  | DAC 1 negative output  |
| VOUT2P               | 33  | AIO  | DAC 2 positive output  |
| VOUT2N               | 34  | AIO  | DAC 2 negative output  |
| VOUT3P               | 35  | AIO  | DAC 3 positive output  |
| VOUT3N               | 36  | AIO  | DAC 3 negative output  |
| V <sub>DDA(DA)</sub> | 37  | AS   | DAC analog supply voltage  |
| VOUT4P               | 38  | AIO  | DAC 4 positive output  |
| VOUT4N               | 39  | AIO  | DAC 4 negative output  |
| V <sub>SSA(DA)</sub> | 40  | AGND | DAC analog ground  |
| VOUT5P               | 41  | AIO  | DAC 5 positive output  |
| VOUT5N               | 42  | AIO  | DAC 5 negative output  |
| VOUT6P               | 43  | AIO  | DAC 6 positive output  |
| VOUT6N               | 44  | AIO  | DAC 6 negative output  |

[1] See [Table 4](#).

Table 4: Pin types

| Type | Description                                    |
|------|--|
| AGND | analog ground                                  |
| AIO  | analog input and output                        |
| AS   | analog supply                                  |
| DGND | digital ground                                 |
| DI   | digital input                                  |
| DID  | digital input with internal pull-down resistor |
| DIO  | digital input and output                       |

Table 4: Pin types ...continued

| Type | Description  |
|------|--|
| DIS  | digital Schmitt-triggered input                      |
| DO   | digital output                                       |
| DS   | digital supply                                       |
| IIC  | input and open-drain output for I <sup>2</sup> C-bus |

## 8. Functional description

### 8.1 System clock

The UDA1384 operates in slave mode only; this means that in all applications the system must provide either the system clock (the bit clock for the voice ADC) or the word clock.

The audio ADC part, the voice ADC part and the DAC part can operate at different sampling frequencies (DAC-WS and ADC-WS modes) as well as a common frequency (SYSCLK, WSDA and DSD modes).

The voice ADC part supports a sampling frequency up to 50 kHz and the audio ADC supports a sampling frequency up to 100 kHz. The DAC sampling frequency range is extended up to 200 kHz with the range above 100 kHz being supported through 192 kHz sampling mode, which halves the oversampling ratio of SYSCLK and internal clocks.

The mode of operation of the audio and voice channels can be set via the L3-bus or I<sup>2</sup>C-bus microcontroller interface and are summarized in [Table 5](#) and [Table 6](#).

When applied, the system clock must be locked in frequency to the corresponding digital interface clocks.

The voice ADC part can either receive or generate the WSV signal as shown in [Table 6](#).

Table 5: Audio ADC and DAC operating clock mode

| Mode   | Audio ADC |  | Audio DAC |   |
|--------|-----------|--|-----------|---|
|        | Clock     | Frequency  | Clock     | Frequency   |
| SYSCLK | SYSCLK    | 256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub> | SYSCLK    | 256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub>                            |
|        |           |  | SYSCLK    | 128f <sub>s</sub> , 192f <sub>s</sub> , 256f <sub>s</sub> or 384f <sub>s</sub> ;<br>192 kHz sampling mode |
| DAC-WS | SYSCLK    | 256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub> | WSDA      | 1f <sub>s</sub>   |
| ADC-WS | WSAD      | 1f <sub>s</sub>  | SYSCLK    | 256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub>                            |
|        |           |  | SYSCLK    | 128f <sub>s</sub> , 192f <sub>s</sub> , 256f <sub>s</sub> or 384f <sub>s</sub> ;<br>192 kHz sampling mode |
| WSDA   | WSDA      | 1f <sub>s</sub>  | WSDA      | 1f <sub>s</sub>   |
| DSD    | SYSCLK    | 44.1 kHz × 512   | SYSCLK    | 44.1 kHz × 512  |

Table 6: Voice ADC operating clock mode

| Mode    | Voice ADC   |                   |
|---------|---|-------------------|
|         | Bit clock frequency (BCKV)  | Word select (WSV) |
| WSV-in  | input: 32f <sub>s</sub> , 64f <sub>s</sub> , 128f <sub>s</sub> or 256f <sub>s</sub> | input             |
| WSV-out | input: 32f <sub>s</sub> , 64f <sub>s</sub> , 128f <sub>s</sub> or 256f <sub>s</sub> | output            |

### 8.2 Audio analog-to-digital converter (audio ADC)

The audio analog-to-digital front-end of the UDA1384 consists of 4-channel single-ended ADCs with programmable gain stage (from 0 dB to 24 dB with 3 dB steps), controlled via the microcontroller interface. Using the PGA feature, it is possible to accept an input signal of 900 mV (RMS) or 1.8 V (RMS) if an external resistor of 10 kΩ is used in series. The schematic of audio ADC front-end is shown in [Figure 3](#).

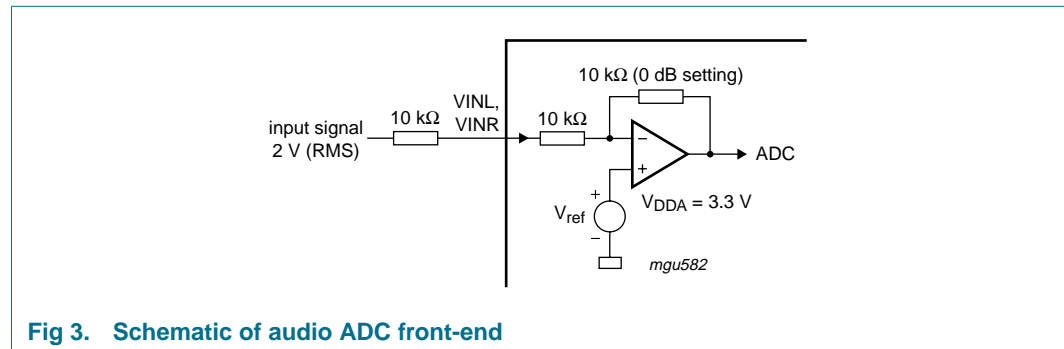


Fig 3. Schematic of audio ADC front-end

### 8.3 Voice Analog-to-Digital Converter (voice ADC)

The voice analog-to-digital front-end of the UDA1384 consists of a single-channel single-ended ADC with a fixed gain (26 dB) Low Noise Amplifier (LNA). Together with the digital variable gain amplification stage, the voice ADC provides optimal processing and reproduction of the microphone signal. The supported sampling frequency range is from 7 kHz to 50 kHz. Power-down of the LNA and the ADC can be controlled separately.

### 8.4 Decimation filter of audio ADC

The decimation from  $64f_s$  is performed in two stages. The first stage realizes  $\left(\frac{\sin x}{x}\right)^4$  characteristics with a decimation factor of 8. The second stage consists of three half-band filters, each decimating by a factor of 2. The filter characteristics are shown in [Table 7](#).

Table 7: Decimation filter characteristics (audio ADC)

| Item             | Condition           | Value (dB) |
|------------------|---------------------|------------|
| Pass-band ripple | $0f_s$ to $0.45f_s$ | $\pm 0.01$ |
| Pass-band droop  | $0.45f_s$           | -0.2       |
| Stop band        | $> 0.55f_s$         | -70        |
| Dynamic range    | $0f_s$ to $0.45f_s$ | $> 135$    |

### 8.5 Decimation filter of voice ADC

The voice ADC decimation filter is realized with the combination of a Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter for shorter group delay. The filter characteristics are shown in [Table 8](#). During the power-on sequence, the output of the ADC is hard muted for a certain period. This hard-mute time can be chosen between 1024 samples and 2048 samples.



**Table 8: Decimation filter characteristics (voice ADC)**

| Item             | Condition           | Value (dB) |
|------------------|---------------------|------------|
| Pass-band ripple | $0f_s$ to $0.45f_s$ | $\pm 0.05$ |
| Pass-band droop  | $0.45f_s$           | $-0.2$     |
| Stop band        | $> 0.55f_s$         | $-65$      |
| Dynamic range    | $0f_s$ to $0.45f_s$ | $> 110$    |

## 8.6 Interpolation filter of DAC

The digital interpolation filter interpolates from  $1f_s$  to  $128f_s$  (or to  $64f_s$  in the 192 kHz sampling mode) by cascading FIR filters, and has two sets of filter coefficients for sharp and slow roll-off as given in [Table 9](#) and [Table 10](#).

**Table 9: Interpolation filter characteristics (sharp roll-off)**

| Item             | Condition           | Value (dB)  |
|------------------|---------------------|-------------|
| Pass-band ripple | $0f_s$ to $0.45f_s$ | $\pm 0.002$ |
| Stop band        | $> 0.55f_s$         | $-75$       |
| Dynamic range    | $0f_s$ to $0.45f_s$ | $> 135$     |

**Table 10: Interpolation filter characteristics (slow roll-off)**

| Item             | Condition           | Value (dB)  |
|------------------|---------------------|-------------|
| Pass-band ripple | $0f_s$ to $0.22f_s$ | $\pm 0.002$ |
| Pass-band droop  | $0.45f_s$           | $-3.1$      |
| Stop band        | $> 0.78f_s$         | $-94$       |
| Dynamic range    | $0f_s$ to $0.22f_s$ | $> 135$     |

## 8.7 Noise shaper of DAC

The 3rd-order noise shaper operates at either  $128f_s$  or  $64f_s$  (in the 192 kHz sampling mode), and converts the 24-bit input signal into a 5-bit signal stream. The noise shaper shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved.

## 8.8 Digital mixer

The UDA1384 has 6 digital mixers inside the interpolator (see [Figure 4](#)). The ADC signals can be mixed with the I<sup>2</sup>S-bus input signals. The mixing of the ADC signals can be selected by the bits MIX[1:0].

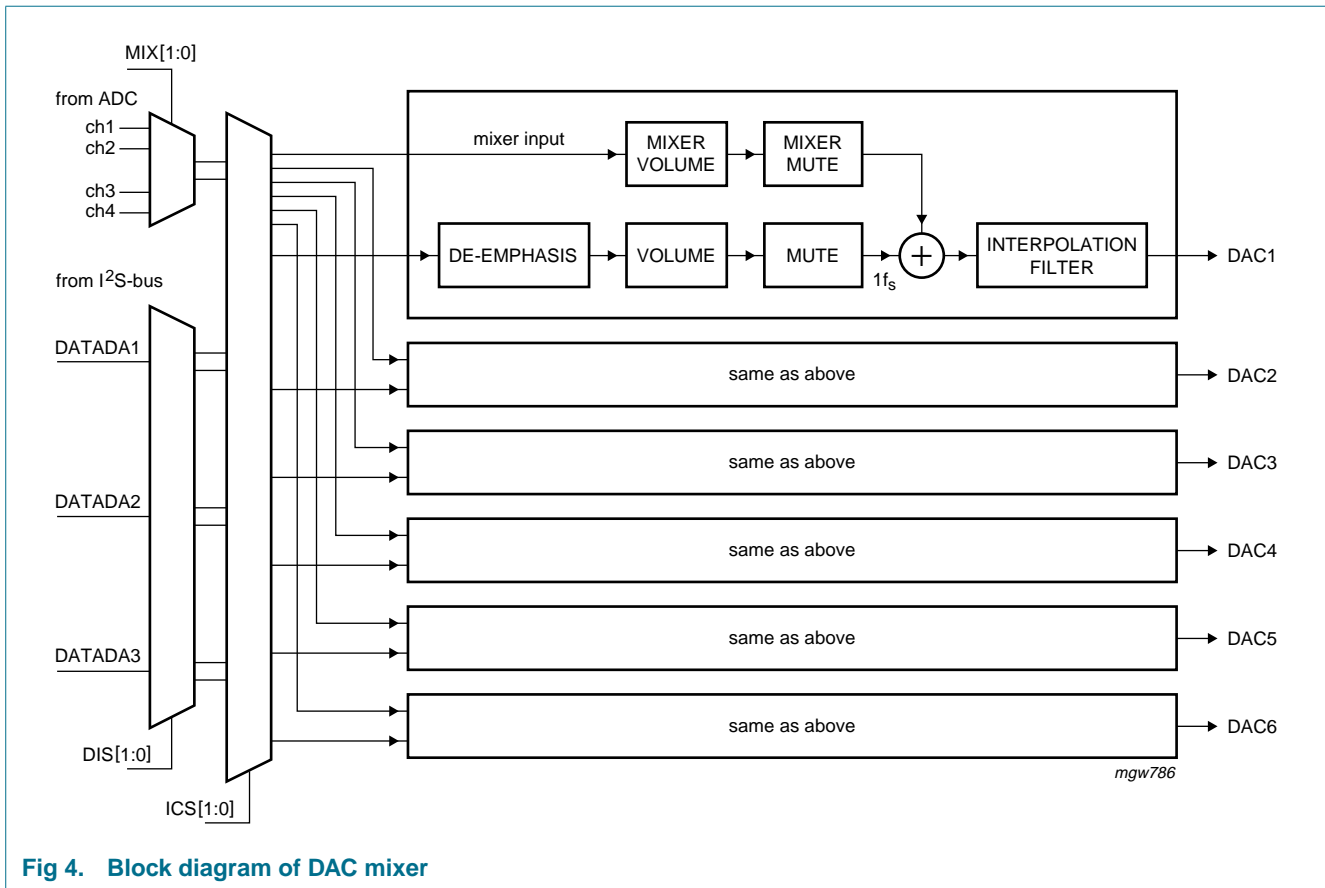


Fig 4. Block diagram of DAC mixer

### 8.9 Audio digital-to-analog converters

The audio digital-to-analog front-end of the UDA1384 consists of 6-channel differential SDACs: an SDAC is a multi-bit DAC based upon switched resistors. To minimize data dependent modulation effects, a Dynamic Element Matching (DEM) algorithm scrambler circuit and DC current compensation circuit are implemented with the SDAC.

### 8.10 Power-on reset

The UDA1384 has an internal power-on reset circuit which initializes the device (see [Figure 5](#)). All the digital sound processing features and the system controlling features are set to their default values in the L3-bus and the I<sup>2</sup>C-bus modes.

The reset time (see [Figure 6](#)) is determined by an external capacitor which is connected between pin V<sub>ref</sub> and ground. The reset time should be at least 250 μs for V<sub>ref</sub> < 1.25 V. When V<sub>DDA(AD)</sub> is switched off, the device will be reset again for V<sub>ref</sub> < 0.75 V.

During the reset time, the system clock should be running.

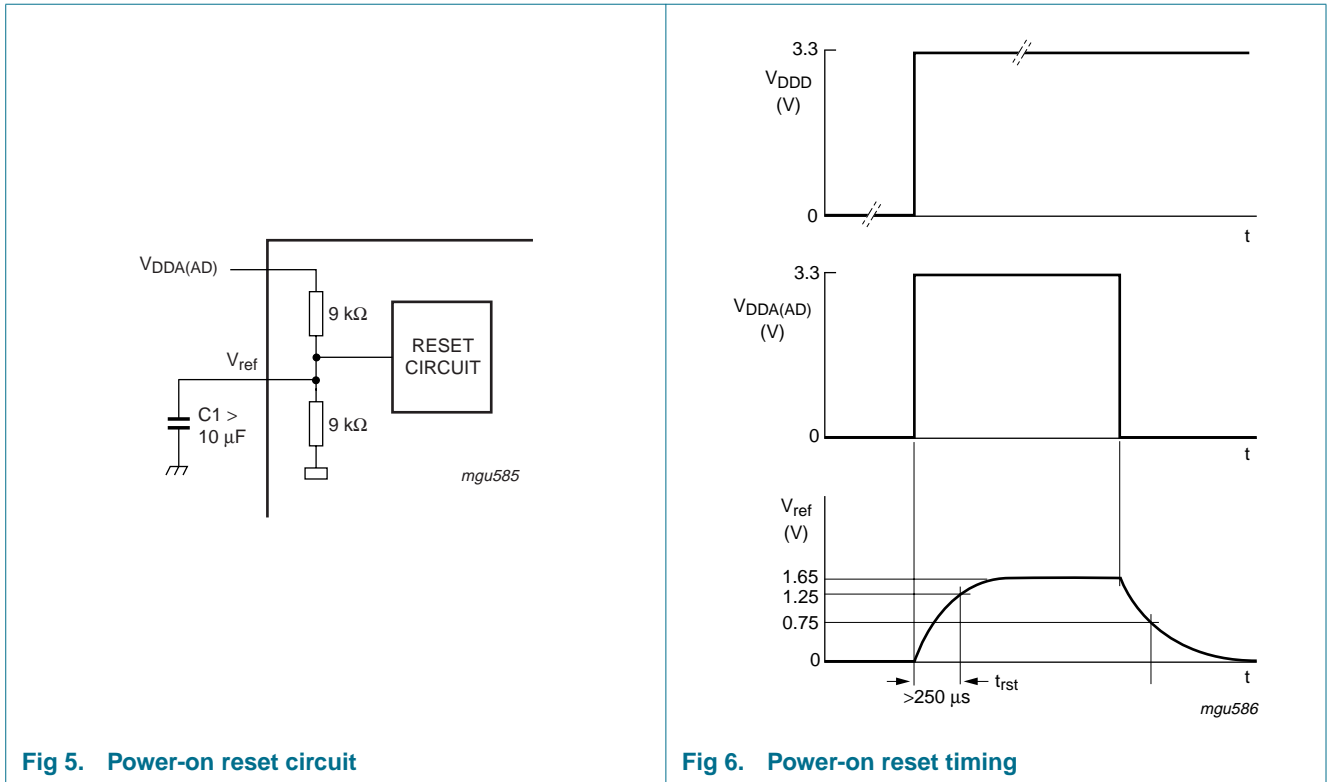


Fig 5. Power-on reset circuit

Fig 6. Power-on reset timing

### 8.11 Audio digital interface

The following audio formats can be selected via the microcontroller interface:

- I<sup>2</sup>S-bus format with data word length of up to 24 bits
- MSB-justified format with data word length of up to 24 bits
- LSB-justified format with data word length of 16 bits, 20 bits or 24 bits
- Multichannel formats with data word length of 20 bits or 24 bits. The used data lines are DATAAD1 and DATADA1 and the sampling frequency must be below 50 kHz

The formats are illustrated in [Figure 7](#) and [Figure 8](#).

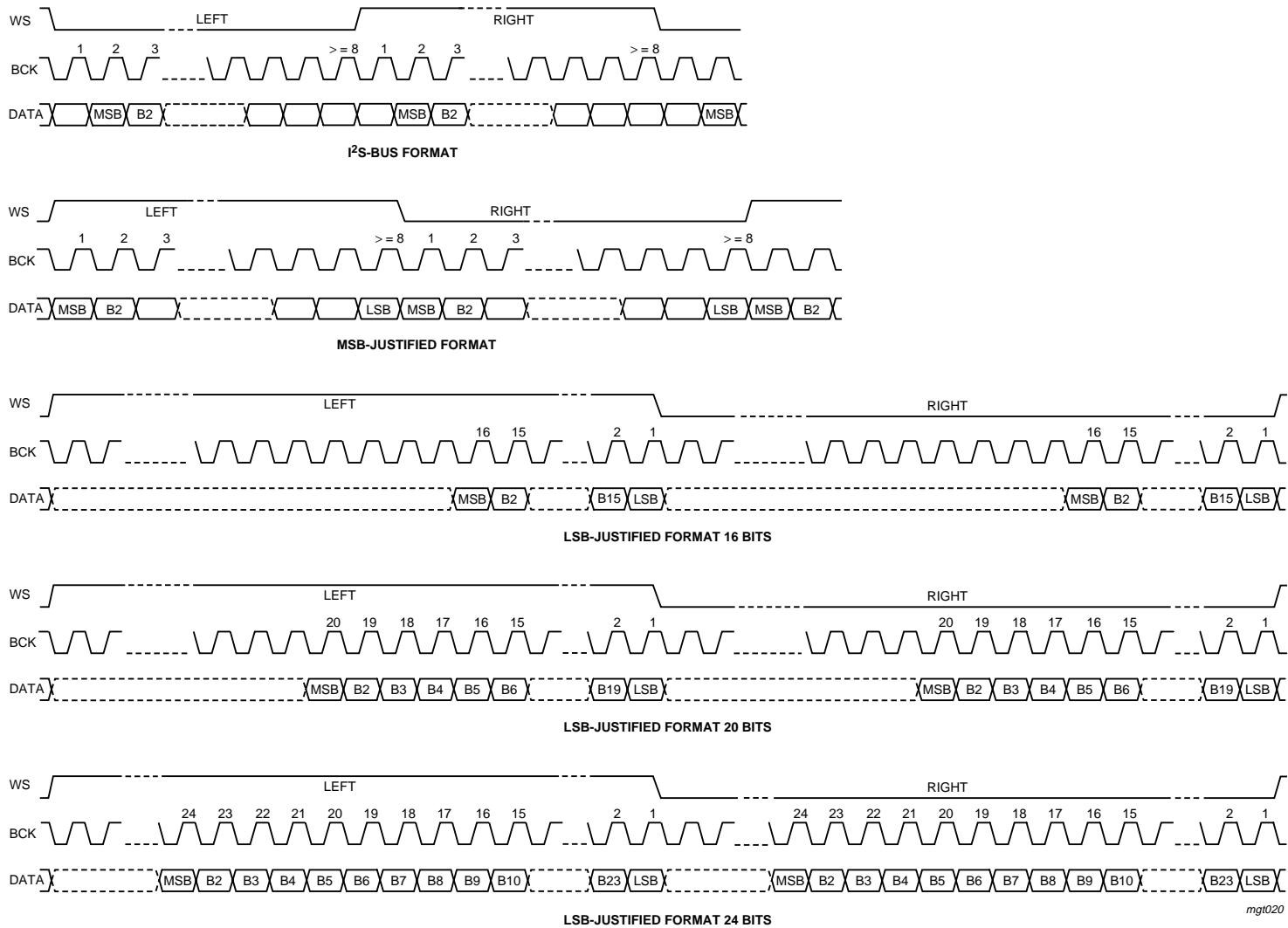
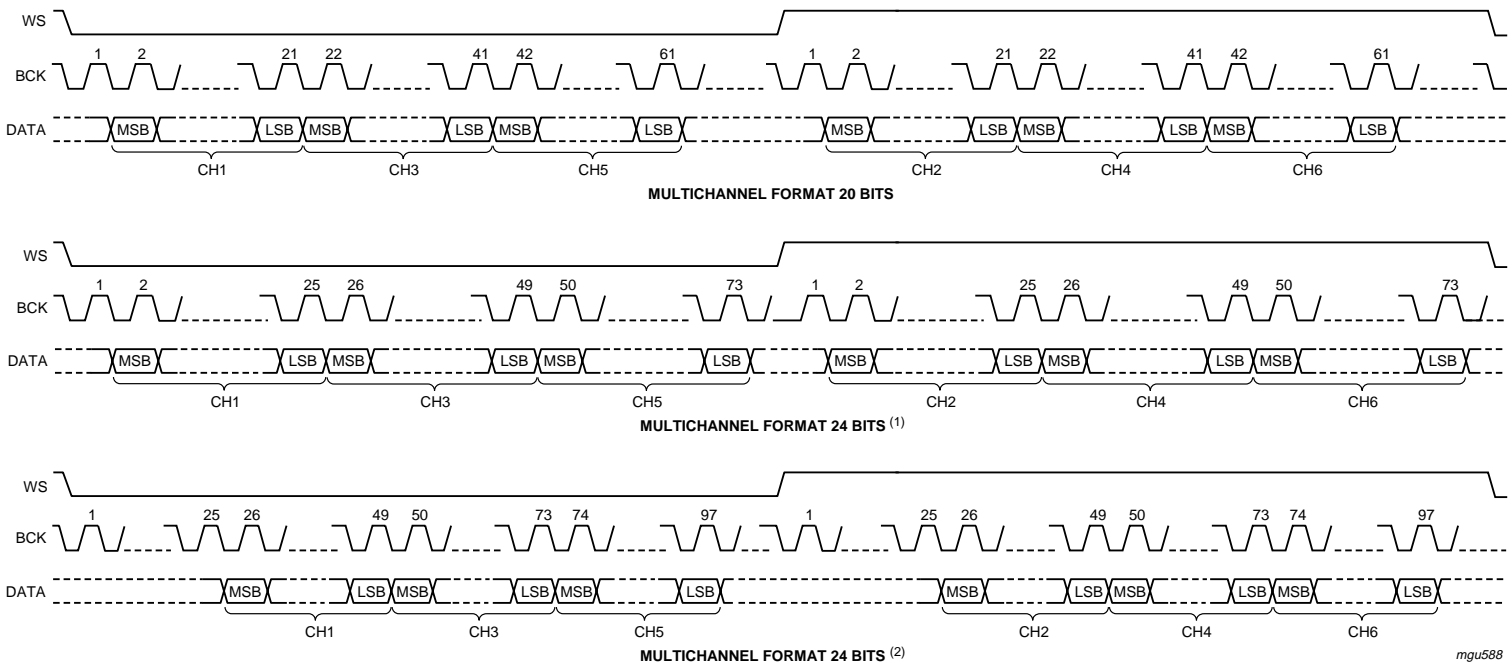


Fig 7. Formats of input and output data (single-channel)



- (1) Format 1.
- (2) Format 2.

Fig 8. Formats of input and output data (multichannel)

mgus88

### 8.12 Voice digital interface

The following voice formats can be selected via the microcontroller interface:

- I<sup>2</sup>S-bus format with data word length of up to 20 bits. The left and the right channels contain the same data.
- Mono channel format with data word length of up to 20 bits.

The formats are illustrated in [Figure 9](#).

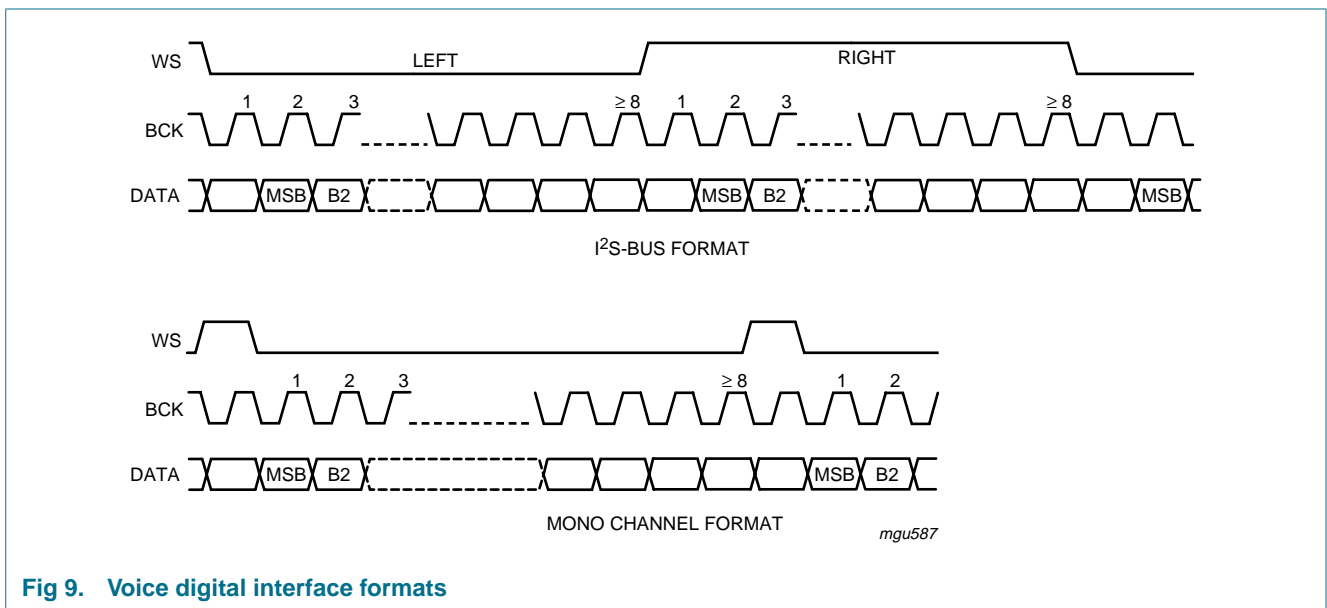


Fig 9. Voice digital interface formats

### 8.13 DSD mode

The UDA1384 can receive 2.8224 MHz DSD signals and generate 88.2 kHz multibit PCM signals as well as analog signal outputs. The configuration of the UDA1384 in the DSD mode is shown in [Figure 10](#).

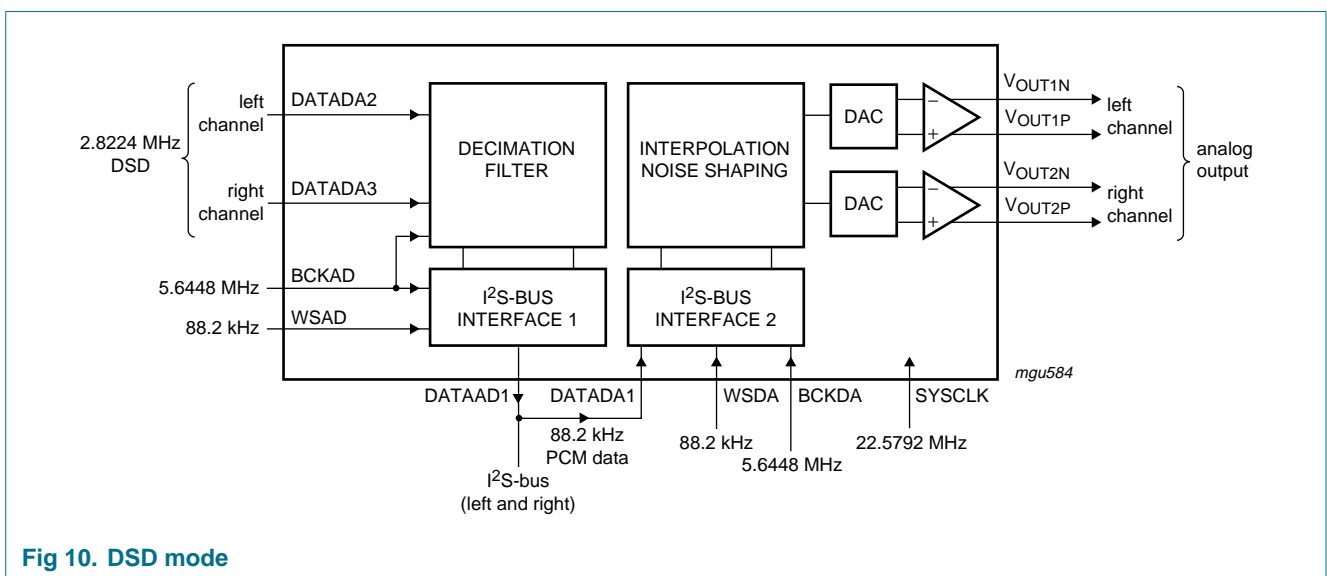


Fig 10. DSD mode

## 8.14 Microcontroller interface mode

The microcontroller interface mode can be selected as shown in [Table 11](#):

- L3-bus mode when pin I2C\_L3 = LOW
- I<sup>2</sup>C-bus mode when pin I2C\_L3 = HIGH

**Table 11: Pin function in the L3-bus or I<sup>2</sup>C-bus mode**

| Pin    | Level on pin I2C_L3 |                                  |
|--------|---------------------|----------------------------------|
|        | LOW                 | HIGH                             |
|        | L3-bus mode signal  | I <sup>2</sup> C-bus mode signal |
| MCCLK  | L3CLOCK             | SCL                              |
| MCDATA | L3DATA              | SDA                              |
| MCMODE | L3MODE              | QMUTE                            |

**Table 12: QMUTE**

| Signal QMUTE | Function  |
|--------------|-----------|
| LOW          | no muting |
| HIGH         | muting    |

All the features are accessible with the I<sup>2</sup>C-bus interface protocol as with the L3-bus interface protocol.

The detailed description of the device operation in the L3-bus mode and I<sup>2</sup>C-bus mode is given in [Section 9](#) and [Section 10](#), respectively.

## 9. L3-bus interface

### 9.1 General

The UDA1384 has an L3-bus microcontroller interface and all the digital sound processing features and various system settings can be controlled by a microcontroller.

The exchange of data and control information between the microcontroller and the UDA1384 is LSB first and is accomplished through a serial hardware L3-bus interface comprising the following pins:

- MCCLK: clock line with signal L3CLOCK
- MCDATA: data line with signal L3DATA
- MCMODE: mode line with signal L3MODE

The L3-bus format has two modes of operation:

- Address mode
- Data transfer mode

The address mode is used to select a device for a subsequent data transfer. The address mode is characterized by signal L3MODE = LOW and a burst of 8 pulses for signal L3CLOCK, accompanied by 8 bits (see [Figure 11](#)).

The data transfer mode is characterized by signal L3MODE = HIGH and is used to transfer one or more bytes representing a register address, instruction or data.

Basically, two types of data transfers can be defined:

- Write action: data transfer **to** the device
- Read action: data transfer **from** the device.

## 9.2 Device addressing

The device address consists of one byte with:

- Data Operating Mode (DOM) bits 0 and 1 representing the type of data transfer (see [Table 13](#))
- Address bits 2 to 7 representing a 6-bit device address. The address of the UDA1384 is 01 0100 (bits 2 to 7).

**Table 13: Selection of data transfer**

| DOM   |       | Transfer                   |
|-------|-------|----------------------------|
| Bit 1 | Bit 0 |                            |
| 0     | 0     | not used                   |
| 0     | 1     | not used                   |
| 1     | 0     | write data or prepare read |
| 1     | 1     | read data                  |

## 9.3 Register addressing

After sending the device address (including DOM bits), indicating whether the information is to be read or written, one data byte is sent using bit 0 to indicate whether the information will be read or written and bits 1 to 7 for the destination register address.

Basically, there are 3 methods for register addressing:

1. Addressing for write data: bit 0 is logic 0 indicating a write action to the destination register, followed by bits 1 to 7 indicating the register address (see [Figure 11](#)).
2. Addressing for prepare read: bit is logic 1, indicating that data will be read from the register (see [Figure 12](#)).
3. Addressing for data read action. Here, the device returns a register address prior to sending data from that register. When bit 0 is logic 0, the register address is valid; when bit 0 is logic 1, the register address is invalid (see [Figure 12](#)).



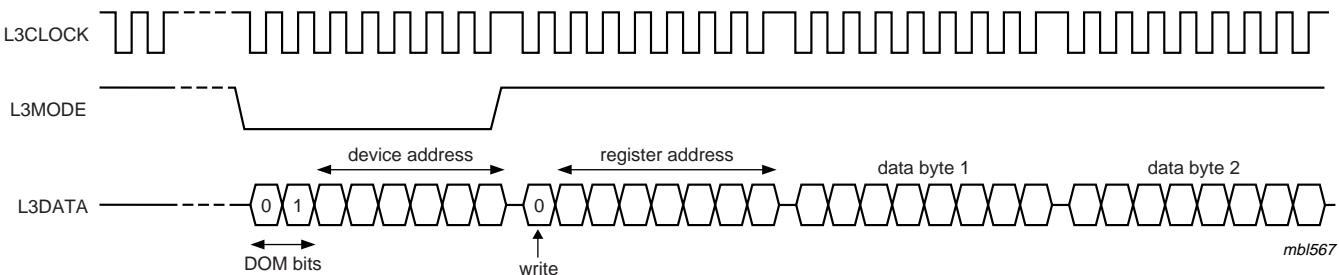


Fig 11. Data write mode

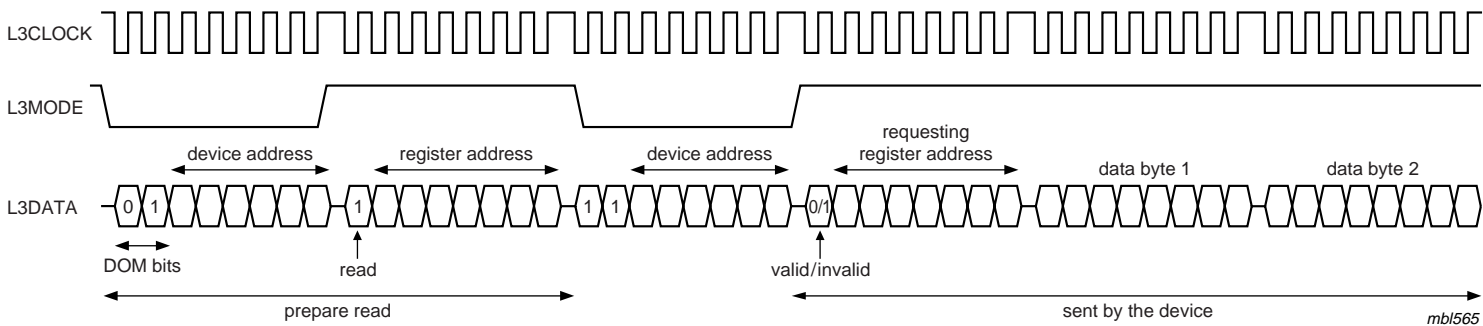


Fig 12. Data read mode

## 9.4 Data write mode

The data write mode is explained in the signal diagram of [Figure 11](#). For writing data to a device, 4 bytes must be sent (see [Table 14](#)):

1. Byte 1 starting with '01' for signalling the write action to the device, followed by the device address '01 0100'
2. Byte 2 starting with a '0' for signalling the write action, followed by 7 bits indicating the destination address in binary format with bit A6 being the MSB and bit A0 being the LSB
3. Byte 3 with bit D15 being the MSB
4. Byte 4 with bit D0 being the LSB

It should be noted that each time a new destination register address needs to be written, the device address must be sent again.

**Table 14: L3-bus write data**

| Byte | L3-bus mode   | Action           | First in time |       |       |       |       |       |       | Latest in time |  |
|------|---------------|------------------|---------------|-------|-------|-------|-------|-------|-------|----------------|--|
|      |               |                  | Bit 0         | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7          |  |
| 1    | address       | device address   | 0             | 1     | 0     | 1     | 0     | 1     | 0     | 0              |  |
| 2    | data transfer | register address | 0             | A6    | A5    | A4    | A3    | A2    | A1    | A0             |  |
| 3    | data transfer | data byte 1      | D15           | D14   | D13   | D12   | D11   | D10   | D9    | D8             |  |
| 4    | data transfer | data byte 2      | D7            | D6    | D5    | D4    | D3    | D2    | D1    | D0             |  |

## 9.5 Data read mode

To read data from the device, a prepare read must first be done and then data read. The data read mode is explained in the signal diagram of [Figure 12](#).

For reading data from a device, the following 6 bytes are involved (see [Table 15](#)):

1. Byte 1 with the device address, including '01' for signalling the write action to the device.
2. Byte 2 is sent with the register address from which data needs to be read. This byte starts with a '1', which indicates that there will be a read action from the register, followed by 7 bits for the destination address in binary format, with bit A6 being the MSB and bit A0 being the LSB.
3. Byte 3 with the device address, including '11' is sent to the device. The '11' indicates that the device must write data to the microcontroller.
4. Byte 4 sent by the device to the bus, with the (requested) register address and a flag bit indicating whether the requested register was valid (bit is logic 0) or invalid (bit is logic 1).
5. Byte 5 sent by the device to the bus, with the data information in binary format, with bit D15 being the MSB.
6. Byte 6 sent by the device to the bus, with the data information in binary format, with bit D0 being the LSB.

Table 15: L3-bus read data

| Byte | L3-bus mode   | Action           | First in time |       |       |       | Latest in time |       |       |       |
|------|---------------|------------------|---------------|-------|-------|-------|----------------|-------|-------|-------|
|      |               |                  | Bit 0         | Bit 1 | Bit 2 | Bit 3 | Bit 4          | Bit 5 | Bit 6 | Bit 7 |
| 1    | address       | device address   | 0             | 1     | 0     | 1     | 0              | 1     | 0     | 0     |
| 2    | data transfer | register address | 1             | A6    | A5    | A4    | A3             | A2    | A1    | A0    |
| 3    | address       | device address   | 1             | 1     | 0     | 1     | 0              | 1     | 0     | 0     |
| 4    | data transfer | register address | 0 or 1        | A6    | A5    | A4    | A3             | A2    | A1    | A0    |
| 5    | data transfer | data byte 1      | D15           | D14   | D13   | D12   | D11            | D10   | D9    | D8    |
| 6    | data transfer | data byte 2      | D7            | D6    | D5    | D4    | D3             | D2    | D1    | D0    |

## 10. I<sup>2</sup>C-bus interface

### 10.1 General

The UDA1384 has an I<sup>2</sup>C-bus microcontroller interface. All the features are accessible with the I<sup>2</sup>C-bus interface protocol. In the I<sup>2</sup>C-bus mode, the DAC mute function is accessible via pin MCMODE with signal QMUTE.

The exchange of data and control information between the microcontroller and the UDA1384 is accomplished through a serial hardware interface comprising the following pins as shown in [Table 11](#):

- MCCLK: clock line with signal SCL
- MCDATA: data line with signal SDA

### 10.2 Characteristics of the I<sup>2</sup>C-bus

The bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to the supply voltage  $V_{DD}$  via a pull-up resistor when connected to the output stages of a microcontroller. For a 400 kHz IC, the recommendation for this type of bus from Philips Semiconductors must be followed (e.g. up to loads of 200 pF on the bus a pull-up resistor can be used, between 200 pF and 400 pF a current source or switched resistor must be used). Data transfer can only be initiated when the bus is not busy.

### 10.3 Bit transfer

One data bit is transferred during each clock pulse (see [Figure 13](#)). The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 400 kHz.

To be able to run on this high frequency, all the inputs and outputs connected to this bus must be designed for this high-speed I<sup>2</sup>C-bus according to the Philips specification.

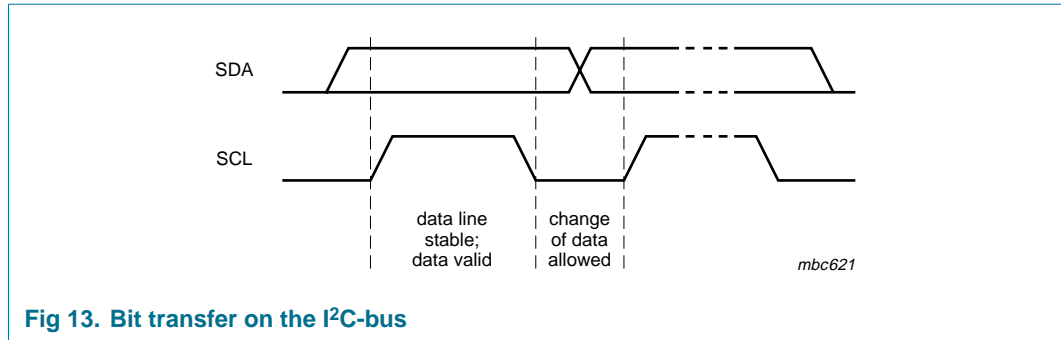


Fig 13. Bit transfer on the I<sup>2</sup>C-bus

### 10.4 Byte transfer

Each byte (8 bits) is transferred with the MSB first (see [Table 16](#)).

Table 16: Byte transfer

| Bit number |   |   |   |     |   |   |   |
|------------|---|---|---|-----|---|---|---|
| MSB        |   |   |   | LSB |   |   |   |
| 7          | 6 | 5 | 4 | 3   | 2 | 1 | 0 |

### 10.5 Data transfer

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves.

### 10.6 Start and stop conditions

Both data and clock line will remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as a start condition (S); see [Figure 14](#). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a stop condition (P).

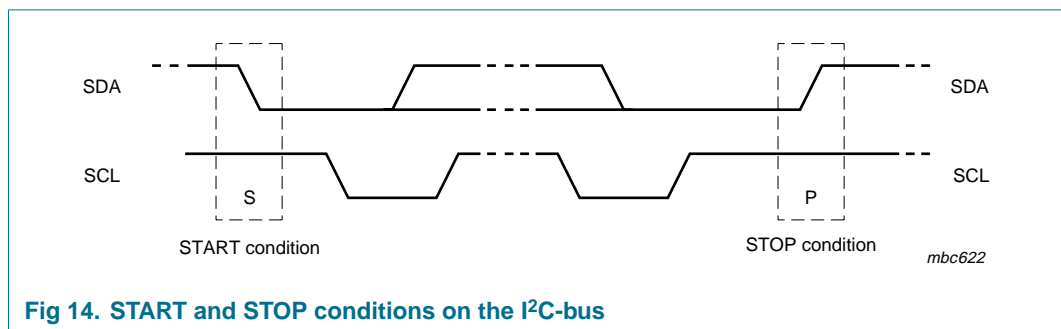


Fig 14. START and STOP conditions on the I<sup>2</sup>C-bus

### 10.7 Acknowledgment

The number of data bits transferred between the start and stop conditions from the transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see [Figure 15](#)). At the acknowledge bit the data line is released by the master and the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed, must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

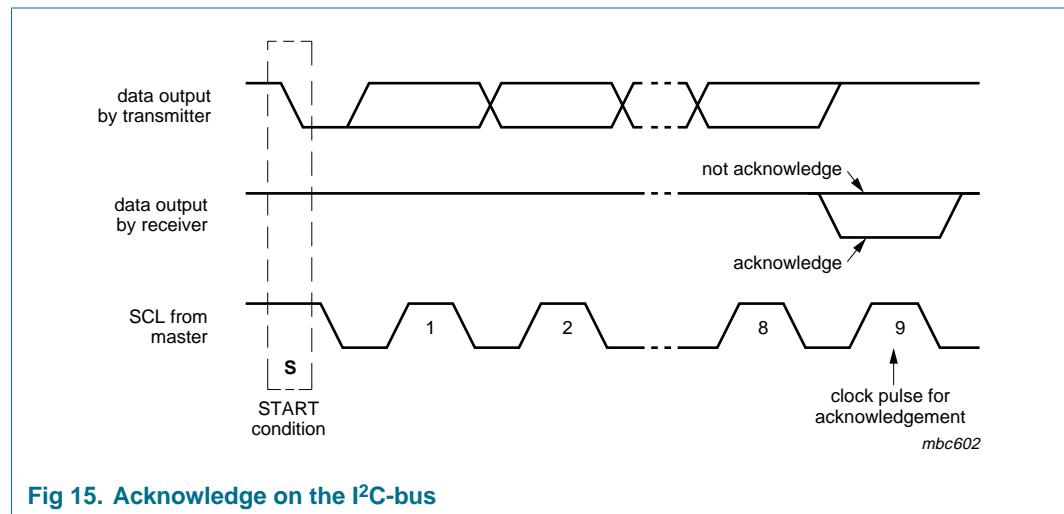


Fig 15. Acknowledge on the I<sup>2</sup>C-bus

### 10.8 Device address

Before any data is transmitted on the I<sup>2</sup>C-bus, the device which should respond is addressed first. The addressing is always done with byte 1 transmitted after the start procedure. The UDA1384 acts as a slave receiver or a slave transmitter.

Therefore, the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The UDA1384 device address is shown in [Table 17](#).

Table 17: I<sup>2</sup>C-bus device address of UDA1384

| Device address |    |    |    |    |    |    | R/W |
|----------------|----|----|----|----|----|----|-----|
| A6             | A5 | A4 | A3 | A2 | A1 | A0 |     |
| 0              | 0  | 1  | 1  | 0  | 0  | 0  | 0/1 |

### 10.9 Register address

The register addresses in the I<sup>2</sup>C-bus mode are the same as in the L3-bus mode. The register addresses are defined in [Section 11](#).

### 10.10 Write and read data

The I<sup>2</sup>C-bus configurations for a write and read cycle are shown in [Table 18](#) and [Table 19](#), respectively.

The write cycle is used to write groups of two bytes to the internal registers for the settings. It is also possible to read the registers for the device status information.

### 10.11 Write cycle

The I<sup>2</sup>C-bus configuration for a write cycle is shown in [Table 18](#). The write cycle is used to write the data to the internal registers. The device and register addresses are one byte each, the setting data is always a pair of two bytes.

The format of the write cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address '0011 000' and a logic 0 (write) for the R/W bit.
3. This is followed by an acknowledge (A) from the UDA1384.
4. After this the microcontroller writes the 8-bit register address (ADDR) where the writing of the register content of the UDA1384 must start.
5. The UDA1384 acknowledges this register address (A).
6. The microcontroller sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the UDA1384.
7. If repeated groups of 2 bytes data are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the UDA1384.
8. Finally, the UDA1384 frees the I<sup>2</sup>C-bus and the microcontroller can generate a stop condition (P).

**Table 18: Master transmitter writes to UDA1384 registers in the I<sup>2</sup>C-bus mode**

|   | Device address | R/W | Register address | Data 1        | Data 2 [1]  | Data n [1]  |   |
|---|----------------|-----|------------------|---------------|-------------|-------------|---|
| S | 0011 000       | 0 A | ADDR             | A MS1 A LS1 A | MS2 A LS2 A | MSn A LSn A | P |

A = acknowledge from UDA1384

[1] Auto increment of register address.

### 10.12 Read cycle

The read cycle is used to read the data values from the internal registers. The I<sup>2</sup>C-bus configuration for a read cycle is shown in [Table 19](#).

The format of the read cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address '0011 000' and a logic 0 (write) for the R/W bit.
3. This is followed by an acknowledge (A) from the UDA1384.
4. After this the microcontroller writes the 8-bit register address (ADDR) where the reading of the register content of the UDA1384 must start.
5. The UDA1384 acknowledges this register address.
6. Then the microcontroller generates a repeated start (Sr).

7. Then the microcontroller generates the device address '0011 000' again, but this time followed by a logic 1 (read) of the R/W bit. An acknowledge is followed from the UDA1384.
8. The UDA1384 sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the microcontroller (master).
9. If repeated groups of 2 bytes are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the microcontroller.
10. The microcontroller stops this cycle by generating a Negative Acknowledge (NA).
11. Finally, the UDA1384 frees the I<sup>2</sup>C-bus and the microcontroller can generate a stop condition (P).

**Table 19: Master transmitter reads from the UDA1384 registers in the I<sup>2</sup>C-bus mode**

|                              | Device address | R/W |   | Register address |   |    | Device address | R/W |   | Data 1                      |   |     |   | Data 2 [1] |   |     |   | Data n [1] |   |     |    |   |
|------------------------------|----------------|-----|---|------------------|---|----|----------------|-----|---|-----------------------------|---|-----|---|------------|---|-----|---|------------|---|-----|----|---|
| S                            | 0011 000       | 0   | A | ADDR             | A | Sr | 0011 000       | 1   | A | MS1                         | A | LS1 | A | MS2        | A | LS2 | A | MSn        | A | LSn | NA | P |
| A = acknowledge from UDA1384 |                |     |   |                  |   |    |                |     |   | A = acknowledge from master |   |     |   |            |   |     |   |            |   |     |    |   |

[1] Auto increment of register address.

## 11. Register mapping

In this chapter the register addressing and mapping of the microcontroller interface of the UDA1384 is given.

In [Table 20](#) an overview of the register mapping is given.

In [Table 21](#) the actual register mapping is given and the register definitions are explained in [Section 11.3](#) to [Section 11.14](#).

### 11.1 Address mapping

**Table 20: Overview of register mapping**

| Address                            | Function                          |
|------------------------------------|-----------------------------------|
| <b>System settings</b>             |                                   |
| 00h                                | system                            |
| 01h                                | audio ADC and DAC subsystem       |
| 02h                                | voice ADC system                  |
| <b>Status (read out registers)</b> |                                   |
| 0Fh                                | status outputs                    |
| <b>Interpolator settings</b>       |                                   |
| 10h                                | DAC channel and feature selection |
| 11h                                | DAC feature control               |
| 12h                                | DAC channel 1                     |
| 13h                                | DAC channel 2                     |
| 14h                                | DAC channel 3                     |
| 15h                                | DAC channel 4                     |

**Table 20: Overview of register mapping** ...continued

| Address                                  | Function                       |
|--|--------------------------------|
| 16h                                      | DAC channel 5                  |
| 17h                                      | DAC channel 6                  |
| 18h                                      | DAC mixing channel 1           |
| 19h                                      | DAC mixing channel 2           |
| 1Ah                                      | DAC mixing channel 3           |
| 1Bh                                      | DAC mixing channel 4           |
| 1Ch                                      | DAC mixing channel 5           |
| 1Dh                                      | DAC mixing channel 6           |
| <b>ADC input amplifier gain settings</b> |                                |
| 20h                                      | audio ADC input amplifier gain |
| 21h                                      | voice ADC input amplifier gain |
| <b>Supplemental settings</b>             |                                |
| 30h                                      | supplemental settings 1        |
| 31h                                      | supplemental settings 2        |



## 11.2 Register mapping

Table 21: UDA1384 register mapping [1]

| Add                           | Function                          | D15     | D14  | D13  | D12 | D11 | D10  | D9   | D8   | D7   | D6   | D5  | D4   | D3   | D2   | D1   | D0   |
|-------------------------------|-----------------------------------|---------|------|------|-----|-----|------|------|------|------|------|-----|------|------|------|------|------|
| <b>System settings</b>        |                                   |         |      |      |     |     |      |      |      |      |      |     |      |      |      |      |      |
| 00h                           | system                            | RST [2] | VFS1 | VFS0 | VCE | VAP | DSD  | SC1  | SC0  | OP1  | OP0  | FS1 | FS0  | ACE  | ADP  | DCE  | DAP  |
|                               |                                   | -       | 0    | 0    | 1   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 1    | 1    | 0    | 1    | 0    |
| 01h                           | audio ADC and DAC subsystem       | DC      | PAB  | PAA  | MTB | MTA | AIF2 | AIF1 | AIF0 | DAG  | FIL  | DVD | DIS1 | DIS0 | DIF2 | DIF1 | DIF0 |
|                               |                                   | 1       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |
| 02h                           | voice ADC system                  | -       | -    | -    | -   | -   | -    | -    | -    | BCK1 | BCK0 | WSM | VH1  | VH0  | PVA  | MTV  | VIF  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 1    | 1   | 0    | 1    | 0    | 0    | 0    |
| <b>Status (read out only)</b> |                                   |         |      |      |     |     |      |      |      |      |      |     |      |      |      |      |      |
| 0Fh                           | status outputs                    | -       | -    | -    | -   | -   | -    | -    | -    | -    | -    | VS  | AS1  | AS0  | DS2  | DS1  | DS0  |
| <b>Interpolator settings</b>  |                                   |         |      |      |     |     |      |      |      |      |      |     |      |      |      |      |      |
| 10h                           | DAC channel and feature selection | MIX1    | MIX0 | MC5  | MC4 | MC3 | MC2  | MC1  | MC0  | SEL1 | SEL0 | CS5 | CS4  | CS3  | CS2  | CS1  | CS0  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |
| 11h                           | DAC feature control               | ICS1    | ICS0 | DE2  | DE1 | DE0 | PD   | MT   | QM   | VC7  | VC6  | VC5 | VC4  | VC3  | VC2  | VC1  | VC0  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |
| 12h                           | DAC channel 1                     | ICS1    | ICS0 | DE2  | DE1 | DE0 | PD   | MT   | QM   | VC7  | VC6  | VC5 | VC4  | VC3  | VC2  | VC1  | VC0  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |
| 13h                           | DAC channel 2                     | -       | -    | DE2  | DE1 | DE0 | PD   | MT   | QM   | VC7  | VC6  | VC5 | VC4  | VC3  | VC2  | VC1  | VC0  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |
| 14h                           | DAC channel 3                     | ICS1    | ICS0 | DE2  | DE1 | DE0 | PD   | MT   | QM   | VC7  | VC6  | VC5 | VC4  | VC3  | VC2  | VC1  | VC0  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |
| 15h                           | DAC channel 4                     | -       | -    | DE2  | DE1 | DE0 | PD   | MT   | QM   | VC7  | VC6  | VC5 | VC4  | VC3  | VC2  | VC1  | VC0  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |
| 16h                           | DAC channel 5                     | ICS1    | ICS0 | DE2  | DE1 | DE0 | PD   | MT   | QM   | VC7  | VC6  | VC5 | VC4  | VC3  | VC2  | VC1  | VC0  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |
| 17h                           | DAC channel 6                     | -       | -    | DE2  | DE1 | DE0 | PD   | MT   | QM   | VC7  | VC6  | VC5 | VC4  | VC3  | VC2  | VC1  | VC0  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |
| 18h                           | DAC mixing channel 1              | ICS1    | ICS0 | -    | -   | -   | PD   | MT   | QM   | VC7  | VC6  | VC5 | VC4  | VC3  | VC2  | VC1  | VC0  |
|                               |                                   | 0       | 0    | 0    | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0   | 0    | 0    | 0    | 0    | 0    |

**Table 21: UDA1384 register mapping [1] ...continued**

| Add                                      | Function                             | D15       | D14       | D13    | D12    | D11      | D10      | D9       | D8       | D7       | D6         | D5         | D4         | D3       | D2       | D1        | D0         |
|--|--------------------------------------|-----------|-----------|--------|--------|----------|----------|----------|----------|----------|------------|------------|------------|----------|----------|-----------|------------|
| 19h                                      | DAC mixing channel 2                 | -<br>0    | -<br>0    | -<br>0 | -<br>0 | -<br>0   | PD<br>0  | MT<br>0  | QM<br>0  | VC7<br>0 | VC6<br>0   | VC5<br>0   | VC4<br>0   | VC3<br>0 | VC2<br>0 | VC1<br>0  | VC0<br>0   |
| 1Ah                                      | DAC mixing channel 3                 | ICS1<br>0 | ICS0<br>0 | -<br>0 | -<br>0 | -<br>0   | PD<br>0  | MT<br>0  | QM<br>0  | VC7<br>0 | VC6<br>0   | VC5<br>0   | VC4<br>0   | VC3<br>0 | VC2<br>0 | VC1<br>0  | VC0<br>0   |
| 1Bh                                      | DAC mixing channel 4                 | -<br>0    | -<br>0    | -<br>0 | -<br>0 | -<br>0   | PD<br>0  | MT<br>0  | QM<br>0  | VC7<br>0 | VC6<br>0   | VC5<br>0   | VC4<br>0   | VC3<br>0 | VC2<br>0 | VC1<br>0  | VC0<br>0   |
| 1Ch                                      | DAC mixing channel 5                 | ICS1<br>0 | ICS0<br>0 | -<br>0 | -<br>0 | -<br>0   | PD<br>0  | MT<br>0  | QM<br>0  | VC7<br>0 | VC6<br>0   | VC5<br>0   | VC4<br>0   | VC3<br>0 | VC2<br>0 | VC1<br>0  | VC0<br>0   |
| 1Dh                                      | DAC mixing channel 6                 | -<br>0    | -<br>0    | -<br>0 | -<br>0 | -<br>0   | PD<br>0  | MT<br>0  | QM<br>0  | VC7<br>0 | VC6<br>0   | VC5<br>0   | VC4<br>0   | VC3<br>0 | VC2<br>0 | VC1<br>0  | VC0<br>0   |
| <b>ADC input amplifier gain settings</b> |                                      |           |           |        |        |          |          |          |          |          |            |            |            |          |          |           |            |
| 20h                                      | ADC 1 and ADC 2 input amplifier gain | -<br>0    | -<br>0    | -<br>0 | -<br>0 | IB3<br>0 | IB2<br>0 | IB1<br>0 | IB0<br>0 | -<br>0   | -<br>0     | -<br>0     | -<br>0     | IA3<br>0 | IA2<br>0 | IA1<br>0  | IA0<br>0   |
| 21h                                      | voice ADC input amplifier gain       | -<br>-    | -<br>-    | -<br>- | -<br>- | -<br>-   | -<br>-   | -<br>-   | -<br>0   | -<br>0   | -<br>0     | -<br>0     | IV4<br>0   | IV3<br>0 | IV2<br>0 | IV1<br>0  | IV0<br>0   |
| <b>Supplemental settings</b>             |                                      |           |           |        |        |          |          |          |          |          |            |            |            |          |          |           |            |
| 30h                                      | supplemental settings 1              | -<br>0    | -<br>0    | -<br>0 | -<br>0 | -<br>0   | -<br>0   | -<br>0   | -<br>0   | PDT<br>0 | -<br>0     | -<br>0     | -<br>0     | -<br>0   | -<br>0   | -<br>0    | -<br>0     |
| 31h                                      | supplemental settings 2              | -<br>0    | -<br>0    | -<br>0 | -<br>0 | -<br>0   | -<br>0   | -<br>0   | -<br>0   | -<br>0   | DITH2<br>0 | DITH1<br>0 | DITH0<br>0 | -<br>0   | -<br>0   | VMTP<br>0 | PDLNA<br>0 |

- [1] When writing new settings via the L3-bus interface, the default values should always be set to warrant correct operation. Read access to the DAC features register 11h will not return valid data.
- [2] When bit RST is set to logic 1, the default values are set to all the registers as shown in [Table 21](#). When start-up, all the registers in 00h are initialized as the default values and the mute control bits MTA, MTB, MTV, MT and QM are set to logic 1. All other registers have non fixed values.

### 11.3 System settings

Table 22: System register (address 00h) bit allocation

| Bit    | 15             | 14   | 13   | 12  | 11  | 10  | 9   | 8   |
|--------|----------------|------|------|-----|-----|-----|-----|-----|
| Symbol | RST            | VFS1 | VFS0 | VCE | VAP | DSD | SC1 | SC0 |
| Reset  | -              | 0    | 0    | 1   | 0   | 0   | 0   | 0   |
| Access | read and write |      |      |     |     |     |     |     |
| Bit    | 7              | 6    | 5    | 4   | 3   | 2   | 1   | 0   |
| Symbol | OP1            | OP0  | FS1  | FS0 | ACE | ADP | DCE | DAP |
| Reset  | 0              | 0    | 0    | 1   | 1   | 0   | 1   | 0   |
| Access | read and write |      |      |     |     |     |     |     |

Table 23: Description of system register bits

| Bit      | Symbol   | Description  |
|----------|----------|--|
| 15       | RST      | <b>Reset.</b> Bit RST initializes the L3-bus registers with the default settings.<br>1 = Reset to default settings<br>0 = No reset   |
| 14 to 13 | VFS[1:0] | <b>Voice ADC sampling frequency.</b> A 2-bit value to select the voice ADC sampling frequency. Default 00. See <a href="#">Table 24</a> .  |
| 12       | VCE      | <b>Voice ADC clock enable.</b><br>1 = clock enabled (default)<br>0 = clock disabled  |
| 11       | VAP      | <b>Voice ADC power control.</b> Bit VAP is to reduce the power consumption of the voice ADC.<br>1 = state is power-on<br>0 = state is power-off (default)  |
| 10       | DSD      | <b>DSD mode selection.</b> Bit DSD selects the DSD mode.<br>1 = DSD mode<br>0 = normal mode (default)  |
| 9 to 8   | SC[1:0]  | <b>System clock frequency.</b> A 2-bit value to select the used external clock frequency. $128f_s$ system clock for the DAC can be used by setting bit DVD = 1. Default 00. See <a href="#">Table 25</a> . |
| 7 to 6   | OP[1:0]  | <b>Operating mode selection.</b> A 2-bit value to select the operation mode of the audio ADC and DAC. Default 00. See <a href="#">Table 26</a> .   |
| 5 to 4   | FS[1:0]  | <b>Sampling frequency.</b> A 2-bit value to select the sampling frequency of the audio ADC and DAC in the WS mode. Default 01. See <a href="#">Table 27</a> .  |
| 3        | ACE      | <b>ADC clock enable.</b> Bit ACE enables the audio ADC clock<br>1 = clock enabled (default)<br>0 = clock disabled  |
| 2        | ADP      | <b>ADC power control.</b> Bit ADP is to reduce the power consumption of the audio ADC.<br>1 = state is power-on<br>0 = state is power-off (default)  |

**Table 23: Description of system register bits ...continued**

| Bit | Symbol | Description   |
|-----|--------|---|
| 1   | DCE    | <b>DAC clock enable.</b> Bit DCE enables the DAC clock.<br>1 = clock enabled (default)<br>0 = clock disabled                                  |
| 0   | DAP    | <b>DAC power control.</b> Bit DAP is to reduce the power consumption of the DAC.<br>1 = state is power-on<br>0 = state is power-off (default) |

**Table 24: Voice ADC sampling frequency bits**

| VFS1 | VFS0 | Function                       |
|------|------|--------------------------------|
| 0    | 0    | 6.25 kHz to 12.5 kHz (default) |
| 0    | 1    | 12.5 kHz to 25 kHz             |
| 1    | 0    | 25 kHz to 50 kHz               |
| 1    | 1    | reserved                       |

**Table 25: System clock frequency bits**

| SC1 | SC0 | ADC               | DAC               |                   | Remark  |
|-----|-----|-------------------|-------------------|-------------------|---------|
|     |     |                   | Bit DVD = 0       | Bit DVD = 1       |         |
| 0   | 0   | 256f <sub>s</sub> | 256f <sub>s</sub> | 128f <sub>s</sub> | default |
| 0   | 1   | 384f <sub>s</sub> | 384f <sub>s</sub> | 192f <sub>s</sub> |         |
| 1   | 0   | 512f <sub>s</sub> | 512f <sub>s</sub> | 256f <sub>s</sub> |         |
| 1   | 1   | 768f <sub>s</sub> | 768f <sub>s</sub> | 384f <sub>s</sub> |         |

**Table 26: Operating mode bits**

| OP1 | OP0 | ADC mode  | DAC mode  | Remark  |
|-----|-----|---|---|---------|
| 0   | 0   | SYCLK (256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub> ) | SYCLK (128f <sub>s</sub> , 256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub> ) | default |
| 0   | 1   | SYCLK (256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub> ) | WSDA (1f <sub>s</sub> )   |         |
| 1   | 0   | WSAD (1f <sub>s</sub> )   | SYCLK (128f <sub>s</sub> , 256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub> ) |         |
| 1   | 1   | WSDA (1f <sub>s</sub> )   | WSDA (1f <sub>s</sub> )   |         |

**Table 27: Audio ADC and DAC sampling frequency bits**

| FS1 | FS0 | Function                   |
|-----|-----|----------------------------|
| 0   | 0   | 12.5 kHz to 25 kHz         |
| 0   | 1   | 25 kHz to 50 kHz (default) |
| 1   | 0   | 50 kHz to 100 kHz          |
| 1   | 1   | 100 kHz to 200 kHz         |

## 11.4 Audio ADC and DAC subsystem settings

**Table 28: Audio ADC and DAC subsystem register (address 01h) bit allocation**

| Bit    | 15             | 14  | 13  | 12   | 11   | 10   | 9    | 8    |
|--------|----------------|-----|-----|------|------|------|------|------|
| Symbol | DC             | PAB | PAA | MTB  | MTA  | AIF2 | AIF1 | AIF0 |
| Reset  | 1              | 0   | 0   | 0    | 0    | 0    | 0    | 0    |
| Access | read and write |     |     |      |      |      |      |      |
| Bit    | 7              | 6   | 5   | 4    | 3    | 2    | 1    | 0    |
| Symbol | DAG            | FIL | DVD | DIS1 | DIS0 | DIF2 | DIF1 | DIF0 |
| Reset  | 0              | 0   | 0   | 0    | 0    | 0    | 0    | 0    |
| Access | read and write |     |     |      |      |      |      |      |

**Table 29: Description of the audio ADC and DAC subsystem register bit**

| Bit     | Symbol   | Description  |
|---------|----------|--|
| 15      | DC       | <b>ADC DC-filter.</b> Bit DC enables the digital DC-filter of the ADC.<br>1 = DC-filtering is active (default)<br>0 = no DC-filtering  |
| 14      | PAB      | <b>Polarity ADC 2 control.</b> Bit PAB controls the ADC 2 polarity.<br>1 = polarity is inverted<br>0 = polarity is not-inverted (default)  |
| 13      | PAA      | <b>Polarity ADC 1 control.</b> Bit PAA controls the ADC 1 polarity.<br>1 = polarity is inverted<br>0 = polarity is not-inverted (default)  |
| 12      | MTB      | <b>Mute ADC 2.</b> Bit MTB enables the digital mute of ADC 2.<br>1 = ADC 2 is soft muted<br>0 = ADC 2 is not muted (default)   |
| 11      | MTA      | <b>Mute ADC 1.</b> Bit MTA enables the digital mute of ADC 1.<br>1 = ADC 1 is soft muted<br>0 = ADC 1 is not muted (default)   |
| 10 to 8 | AIF[2:0] | <b>ADC output data interface format.</b> A 3-bit value to select the used data format to the I <sup>2</sup> S-bus ADC output interface. Default 000. See <a href="#">Table 30</a> .  |
| 7       | DAG      | <b>DAC gain switch.</b> Bit DAG selects the DAC gain.<br>1 = gain = 6 dB<br>0 = gain = 0 dB (default)  |
| 6       | FIL      | <b>Filter selection.</b> Bit FIL selects the interpolation filter characteristics.<br>1 = slow roll-off<br>0 = sharp roll-off (default)  |
| 5       | DVD      | <b>192 kHz sampling mode selection.</b> Bit DVD selects the oversampling rate of the noise shaper.<br>1 = 64f <sub>s</sub> rate; used for 192 kHz and 176.4 kHz sampling frequencies<br>0 = 128f <sub>s</sub> rate (default) |
| 4 to 3  | DIS[1:0] | <b>Data interface selection.</b> A 2-bit value to select the data interface connection. Default 00. See <a href="#">Table 31</a> .   |
| 2 to 0  | DIF[2:0] | <b>DAC input data interface format.</b> A 3-bit value to select the used data format to the I <sup>2</sup> S-bus DAC input interface. Default 000. See <a href="#">Table 30</a> .  |

Table 30: Data interface format bits

| AIF2 | AIF1 | AIF0 | Function                                |
|------|------|------|---|
| DIF2 | DIF1 | DIF0 |   |
| 0    | 0    | 0    | I <sup>2</sup> S-bus format (default)   |
| 0    | 0    | 1    | LSB-justified format, 16 bits           |
| 0    | 1    | 0    | LSB-justified format, 20 bits           |
| 0    | 1    | 1    | LSB-justified format, 24 bits           |
| 1    | 0    | 0    | MSB-justified format                    |
| 1    | 0    | 1    | multichannel format, 20 bits            |
| 1    | 1    | 0    | multichannel format, 24 bits (format 1) |
| 1    | 1    | 1    | multichannel format, 24 bits (format 2) |

Table 31: Data interface selection bits

| DIS1 | DIS0 | Input to DAC   |
|------|------|--|
| 0    | 0    | DATADA1 to DAC channel 1 and 2, DATADA2 to DAC channel 3 and 4, and DATADA3 to DAC channel 5 and 6 (default) |
| 0    | 1    | DATADA1 to DAC channels 1 to 6   |
| 1    | 0    | DATADA2 to DAC channels 1 to 6   |
| 1    | 1    | DATADA3 to DAC channels 1 to 6   |

## 11.5 Voice ADC system settings

Table 32: Voice ADC system register (address 02h) bit allocation

| Bit    | 15             | 14   | 13  | 12  | 11  | 10  | 9   | 8   |
|--------|----------------|------|-----|-----|-----|-----|-----|-----|
| Symbol | -              | -    | -   | -   | -   | -   | -   | -   |
| Reset  | -              | -    | -   | -   | -   | -   | -   | -   |
| Access | read and write |      |     |     |     |     |     |     |
| Bit    | 7              | 6    | 5   | 4   | 3   | 2   | 1   | 0   |
| Symbol | BCK1           | BCK0 | WSM | VH1 | VH0 | PVA | MTV | VIF |
| Reset  | 0              | 1    | 1   | 0   | 1   | 0   | 0   | 0   |
| Access | read and write |      |     |     |     |     |     |     |

Table 33: Description of the voice ADC system register bits

| Bit     | Symbol   | Description   |
|---------|----------|---|
| 15 to 8 | -        | default 0000 0000   |
| 7 to 6  | BCK[1:0] | <b>BCK frequency of voice ADC.</b> A 2-bit value to select the BCK frequency of the voice ADC in the WSV-out mode. Default 01. See <a href="#">Table 34</a> . |
| 5       | WSM      | <b>WSV mode selection.</b> Bit WSM selects the WSV mode of the voice ADC<br>1 = WSV-in mode (default)<br>0 = WSV-out mode                                     |
| 4 to 3  | VH[1:0]  | <b>Voice ADC high-pass filter setting.</b> A 2-bit value to enable the high-pass filter of the voice ADC. Default 01. See <a href="#">Table 35</a> .          |

Table 33: Description of the voice ADC system register bits ...continued

| Bit | Symbol | Description  |
|-----|--------|--|
| 2   | PVA    | <b>Polarity voice ADC control.</b> Bit PVA controls the voice ADC polarity.<br>1 = polarity is inverted<br>0 = polarity is not-inverted (default)                      |
| 1   | MTV    | <b>Mute voice ADC.</b> Bit MTV enables the digital mute of the voice ADC.<br>1 = ADC 1 is soft muted<br>0 = ADC 1 is not muted (default)                               |
| 0   | VIF    | <b>Voice ADC interface format.</b> Bit VIF selects the data interface format of the voice ADC.<br>1 = mono-channel format<br>0 = I <sup>2</sup> S-bus format (default) |

Table 34: BCK frequency of voice ADC bits

| BCK1 | BCK0 | Function                   |
|------|------|----------------------------|
| 0    | 0    | 32f <sub>s</sub>           |
| 0    | 1    | 64f <sub>s</sub> (default) |
| 1    | 0    | 128f <sub>s</sub>          |
| 1    | 1    | 256f <sub>s</sub>          |

Table 35: Voice ADC high-pass filter setting bits

| VH1 | VH0 | Function   |
|-----|-----|--|
| 0   | 0   | high-pass filter off                             |
| 0   | 1   | f <sub>c</sub> = 0.00008f <sub>s</sub> (default) |
| 1   | 0   | f <sub>c</sub> = 0.0125f <sub>s</sub>            |
| 1   | 1   | f <sub>c</sub> = 0.025f <sub>s</sub>             |

## 11.6 Status output register

Table 36: Status output register (address 0Fh) bit allocation

| Bit    | 15        | 14 | 13 | 12  | 11  | 10  | 9   | 8   |
|--------|-----------|----|----|-----|-----|-----|-----|-----|
| Symbol | -         | -  | -  | -   | -   | -   | -   | -   |
| Reset  | -         | -  | -  | -   | -   | -   | -   | -   |
| Access | read only |    |    |     |     |     |     |     |
| Bit    | 7         | 6  | 5  | 4   | 3   | 2   | 1   | 0   |
| Symbol | -         | -  | VS | AS1 | AS0 | DS2 | DS1 | DS0 |
| Reset  | -         | -  | -  | -   | -   | -   | -   | -   |
| Access | read only |    |    |     |     |     |     |     |

Table 37: Description of status output register bits

| Bit     | Symbol | Description  |
|---------|--------|--|
| 15 to 6 | -      | not used   |
| 5       | VS     | <b>Voice ADC status.</b> Bit VS indicates the hard mute status of the voice ADC.<br>1 = power-down is ready and the clock may be disabled<br>0 = power-down is not ready and the clock should not be disabled                  |
| 4       | AS1    | <b>ADC 2 status.</b> Bit AS1 indicates the hard mute status of ADC 2.<br>1 = power-down is ready and the clock may be disabled<br>0 = power-down is not ready and the clock should not be disabled                             |
| 3       | AS0    | <b>ADC 1 status.</b> Bit AS0 indicates the hard mute status of ADC 1.<br>1 = power-down is ready and the clock may be disabled<br>0 = power-down is not ready and the clock should not be disabled                             |
| 2       | DS2    | <b>DAC channel 5 and 6 status.</b> Bit DS2 indicates the hard mute status of DAC channel 5 and 6.<br>1 = power-down is ready and the clock may be disabled<br>0 = power-down is not ready and the clock should not be disabled |
| 1       | DS1    | <b>DAC channel 3 and 4 status.</b> Bit DS1 indicates the hard mute status of DAC channel 3 and 4.<br>1 = power-down is ready and the clock may be disabled<br>0 = power-down is not ready and the clock should not be disabled |
| 0       | DS0    | <b>DAC channel 1 and 2 status.</b> Bit DS0 indicates the hard mute status of DAC channel 1 and 2.<br>1 = power-down is ready and the clock may be disabled<br>0 = power-down is not ready and the clock should not be disabled |



## 11.7 DAC channel selection

**Table 38: DAC channel select register (address 10h) bit allocation**

| Bit    | 15             | 14   | 13  | 12  | 11  | 10  | 9   | 8   |
|--------|----------------|------|-----|-----|-----|-----|-----|-----|
| Symbol | MIX1           | MIX0 | MC5 | MC4 | MC3 | MC2 | MC1 | MC0 |
| Reset  | 0              | 0    | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |      |     |     |     |     |     |     |
| Bit    | 7              | 6    | 5   | 4   | 3   | 2   | 1   | 0   |
| Symbol | SEL1           | SEL0 | CS5 | CS4 | CS3 | CS2 | CS1 | CS0 |
| Reset  | 0              | 0    | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |      |     |     |     |     |     |     |

**Table 39: Description of DAC channel select register bits**

| Bit      | Symbol   | Description   |
|----------|----------|---|
| 15 to 14 | MIX[1:0] | <b>DAC mixer setting.</b> A 2-bit value to enable the DAC mixer. Default 00. See <a href="#">Table 40</a> .   |
| 13 to 8  | MC[5:0]  | <b>DAC mixing channel selection.</b> A group of 6 enable bits to make DAC mixing channels ready for receiving feature settings through register address 11h. Only selected registers accept new settings. Default 00 0000 (no channel ready). See <a href="#">Table 41</a> .      |
| 7 and 6  | SEL[1:0] | <b>Feature selection.</b> A 2-bit value to select the features to be set through register address 11h. When the feature settings are written, only selected feature settings are changed and non selected features are kept unchanged. Default 00. See <a href="#">Table 42</a> . |
| 5 to 0   | CS[5:0]  | <b>DAC channel selection.</b> A group of 6 enable bits to make DAC channel ready for receiving feature settings through register address 11h. Default 00 0000 (no channel ready). See <a href="#">Table 41</a> .  |

**Table 40: DAC mixer setting bits**

| MIX1 | MIX0 | Function            |
|------|------|---------------------|
| 0    | 0    | no mixing (default) |
| 0    | 1    | no mixing           |
| 1    | 0    | mixing ADC 1        |
| 1    | 1    | mixing ADC 2        |

**Table 41: DAC channel and mixing channel selection bits**

| MC5 | MC4 | MC3 | MC2 | MC1 | MC0 | Function                         |
|-----|-----|-----|-----|-----|-----|----------------------------------|
| CS5 | CS4 | CS3 | CS2 | CS1 | CS0 |                                  |
| 0   | 0   | 0   | 0   | 0   | 0   | no channel ready (default)       |
| 0   | 0   | 0   | 0   | 0   | 1   | channel 1 selected               |
| :   | :   | :   | :   | :   | :   |                                  |
| 0   | 0   | 1   | 0   | 1   | 0   | channel 2 and channel 4 selected |
| :   | :   | :   | :   | :   | :   |                                  |
| 1   | 1   | 1   | 1   | 1   | 1   | all channels selected            |

Table 42: Feature selection bits

| SEL1 | SEL0 | Function  |
|------|------|---|
| 0    | 0    | all features (default)                            |
| 0    | 1    | volume  |
| 1    | 0    | mute and quick mute                               |
| 1    | 1    | de-emphasis, polarity and input channel selection |

## 11.8 DAC features settings

Table 43: DAC features register (address 11h) bit allocation

| Bit    | 15             | 14   | 13  | 12  | 11  | 10  | 9   | 8   |
|--------|----------------|------|-----|-----|-----|-----|-----|-----|
| Symbol | ICS1           | ICS0 | DE2 | DE1 | DE0 | PD  | MT  | QM  |
| Reset  | 0              | 0    | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |      |     |     |     |     |     |     |
| Bit    | 7              | 6    | 5   | 4   | 3   | 2   | 1   | 0   |
| Symbol | VC7            | VC6  | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 |
| Reset  | 0              | 0    | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |      |     |     |     |     |     |     |

Table 44: Description of DAC features register bits

| Bit      | Symbol   | Description   |
|----------|----------|---|
| 15 to 14 | ICS[1:0] | <b>Input channel selection.</b> A 2-bit value to select the input channels. As the controlled channels are paired off, this 2-bit value must be written to each odd channel register. Default 00. See <a href="#">Table 45</a> .                                |
| 13 to 11 | DE[2:0]  | <b>De-emphasis setting.</b> A 3-bit value to enable the digital de-emphasis filter. Default 000. See <a href="#">Table 46</a> .   |
| 10       | PD       | <b>Polarity DAC control.</b> Bit PD controls the DAC polarity.<br>1 = polarity is inverted<br>0 = polarity is not-inverted (default)  |
| 9        | MT       | <b>Muting.</b> Bit MT enables the digital mute. All the DAC outputs are muted at start-up. It is necessary to explicitly switch off for the audio output by means of bit MT.<br>1 = muting (start-up)<br>0 = no muting (default)                                |
| 8        | QM       | <b>Quick mute.</b> Bit QM sets the quick mute mode.<br>1 = quick mute mode<br>0 = soft mute mode (default)  |
| 7 to 0   | VC[7:0]  | <b>Interpolator volume control.</b> An 8-bit value to program the volume attenuation of each channel. The range is from 0 dB to -53 dB in steps of 0.25 dB, from -53 dB to -80 dB in steps of 3 dB and -∞ dB. Default 0000 0000. See <a href="#">Table 47</a> . |

Table 45: Input channel selection bits

| ICS1 | ICS0 | Input to DAC output  |
|------|------|--|
| 0    | 0    | left channel input data to odd channel output; right channel input data to even channel output |
| 0    | 1    | left channel input data to odd and even channel outputs  |
| 1    | 0    | right channel input data to odd and even channel outputs                                       |
| 1    | 1    | left channel input data to even channel output; right channel input data to odd channel output |

Table 46: De-emphasis bits

| DE2 | DE1 | DE0 | Function                 |
|-----|-----|-----|--------------------------|
| 0   | 0   | 0   | no de-emphasis (default) |
| 0   | 0   | 1   | de-emphasis of 32 kHz    |
| 0   | 1   | 0   | de-emphasis of 44.1 kHz  |
| 0   | 1   | 1   | de-emphasis of 48 kHz    |
| 1   | 0   | 0   | de-emphasis of 96 kHz    |
| 1   | 0   | 1   | not used                 |
| 1   | 1   | 0   | not used                 |
| 1   | 1   | 1   | not used                 |

Table 47: Interpolator volume control bits

| VC7 | VC6 | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 | Volume (dB) |
|-----|-----|-----|-----|-----|-----|-----|-----|-------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0 (default) |
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | -0.25       |
| 0   | 0   | 0   | 0   | 0   | 0   | 1   | 0   | -0.50       |
| 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | -0.75       |
| 0   | 0   | 0   | 0   | 0   | 1   | 0   | 0   | -1.00       |
| 0   | 0   | 0   | 0   | 0   | 1   | 0   | 1   | -1.25       |
| :   | :   | :   | :   | :   | :   | :   | :   | :           |
| 1   | 1   | 0   | 1   | 0   | 1   | 0   | 0   | -53         |
| 1   | 1   | 0   | 1   | 1   | 0   | 0   | 0   | -56         |
| 1   | 1   | 0   | 1   | 1   | 1   | 0   | 0   | -59         |
| 1   | 1   | 1   | 0   | 0   | 0   | 0   | 0   | -62         |
| 1   | 1   | 1   | 0   | 0   | 1   | 0   | 0   | -65         |
| 1   | 1   | 1   | 0   | 1   | 0   | 0   | 0   | -68         |
| 1   | 1   | 1   | 0   | 1   | 1   | 0   | 0   | -71         |
| 1   | 1   | 1   | 1   | 0   | 0   | 0   | 0   | -74         |
| 1   | 1   | 1   | 1   | 0   | 1   | 0   | 0   | -77         |
| 1   | 1   | 1   | 1   | 1   | 0   | 0   | 0   | -80         |
| 1   | 1   | 1   | 1   | 1   | 1   | 0   | 0   | -∞          |
| :   | :   | :   | :   | :   | :   | :   | :   | :           |
| 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | -∞          |

## 11.9 DAC channel 1 to channel 6 settings

All the DAC features which are written in register 11h are copied into the odd channel registers.

**Table 48: DAC channel 1, 3 and 5 registers (address 12h, 14h and 16h) bit allocation**

| Bit    | 15             | 14   | 13  | 12  | 11  | 10  | 9   | 8   |
|--------|----------------|------|-----|-----|-----|-----|-----|-----|
| Symbol | ICS1           | ICS0 | DE2 | DE1 | DE0 | PD  | MT  | QM  |
| Reset  | 0              | 0    | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |      |     |     |     |     |     |     |
| Bit    | 7              | 6    | 5   | 4   | 3   | 2   | 1   | 0   |
| Symbol | VC7            | VC6  | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 |
| Reset  | 0              | 0    | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |      |     |     |     |     |     |     |

All the DAC features which are written in register 11h are copied into the even channel registers, except the bits ICS[1:0].

**Table 49: DAC channel 2, 4 and 6 registers (address 13h, 15h and 17h) bit allocation**

| Bit    | 15             | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | -              | -   | DE2 | DE1 | DE0 | PD  | MT  | QM  |
| Reset  | 0              | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |     |     |     |     |     |     |     |
| Bit    | 7              | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Symbol | VC7            | VC6 | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 |
| Reset  | 0              | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |     |     |     |     |     |     |     |

## 11.10 DAC mixing channel settings

All the DAC features which are written in register 11h are copied into the odd mixing channel registers, except the bits DE[2:0].

**Table 50: DAC mixing channel 1, 3 and 5 registers (address 18h, 1Ah and 1Ch) bit allocation**

| Bit    | 15             | 14   | 13  | 12  | 11  | 10  | 9   | 8   |
|--------|----------------|------|-----|-----|-----|-----|-----|-----|
| Symbol | ICS1           | ICS0 | -   | -   | -   | PD  | MT  | QM  |
| Reset  | 0              | 0    | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |      |     |     |     |     |     |     |
| Bit    | 7              | 6    | 5   | 4   | 3   | 2   | 1   | 0   |
| Symbol | VC7            | VC6  | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 |
| Reset  | 0              | 0    | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |      |     |     |     |     |     |     |

All the DAC features which are written in register 11h are copied into the even channel registers, except the bits ICS[1:0] and DE[2:0].

**Table 51: DAC mixing channel 2, 4 and 6 registers (address 19h, 1Bh and 1Dh) bit allocation**

| Bit    | 15             | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|
| Symbol | -              | -   | -   | -   | -   | PD  | MT  | QM  |
| Reset  | 0              | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |     |     |     |     |     |     |     |
| Bit    | 7              | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Symbol | VC7            | VC6 | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 |
| Reset  | 0              | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |     |     |     |     |     |     |     |

## 11.11 Audio ADC 1 and ADC 2 input amplifier gain settings

**Table 52: Audio ADC input amplifier gain register (address 20h) bit allocation**

| Bit    | 15             | 14 | 13 | 12 | 11  | 10  | 9   | 8   |
|--------|----------------|----|----|----|-----|-----|-----|-----|
| Symbol | -              | -  | -  | -  | IB3 | IB2 | IB1 | IB0 |
| Reset  | 0              | 0  | 0  | 0  | 0   | 0   | 0   | 0   |
| Access | read and write |    |    |    |     |     |     |     |
| Bit    | 7              | 6  | 5  | 4  | 3   | 2   | 1   | 0   |
| Symbol | -              | -  | -  | -  | IA3 | IA2 | IA1 | IA0 |
| Reset  | 0              | 0  | 0  | 0  | 0   | 0   | 0   | 0   |
| Access | read and write |    |    |    |     |     |     |     |

**Table 53: Description of audio ADC input amplifier gain register bits**

| Bit      | Symbol  | Description  |
|----------|---------|--|
| 15 to 12 | -       | default 0000   |
| 11 to 8  | IB[3:0] | <b>Audio ADC 2 input amplifier gain.</b> A 4-bit value to program the input amplifier gain in steps of 3 dB (9 settings). Default 0000. See <a href="#">Table 54</a> . |
| 7 to 4   | -       | default 0000   |
| 3 to 0   | IA[3:0] | <b>Audio ADC 1 input amplifier gain.</b> A 4-bit value to program the input amplifier gain in steps of 3 dB (9 settings). Default 0000. See <a href="#">Table 54</a> . |

**Table 54: Audio ADC input amplifier gain bits**

| IA3 | IA2 | IA1 | IA0 | Gain (dB)   |
|-----|-----|-----|-----|-------------|
| IB3 | IB2 | IB1 | IB0 |             |
| 0   | 0   | 0   | 0   | 0 (default) |
| 0   | 0   | 0   | 1   | +3          |
| 0   | 0   | 1   | 0   | +6          |
| 0   | 0   | 1   | 1   | +9          |
| 0   | 1   | 0   | 0   | +12         |
| 0   | 1   | 0   | 1   | +15         |

Table 54: Audio ADC input amplifier gain bits ...continued

| IA3 | IA2 | IA1 | IA0 | Gain (dB) |
|-----|-----|-----|-----|-----------|
| IB3 | IB2 | IB1 | IB0 |           |
| 0   | 1   | 1   | 0   | +18       |
| 0   | 1   | 1   | 1   | +21       |
| 1   | 0   | 0   | 0   | +24       |

### 11.12 Voice ADC gain settings

Table 55: Voice ADC input amplifier gain register (address 21h) bit allocation

| Bit    | 15             | 14 | 13 | 12  | 11  | 10  | 9   | 8   |
|--------|----------------|----|----|-----|-----|-----|-----|-----|
| Symbol | -              | -  | -  | -   | -   | -   | -   | -   |
| Reset  | -              | -  | -  | -   | -   | -   | -   | -   |
| Access | read and write |    |    |     |     |     |     |     |
| Bit    | 7              | 6  | 5  | 4   | 3   | 2   | 1   | 0   |
| Symbol | -              | -  | -  | IV4 | IV3 | IV2 | IV1 | IV0 |
| Reset  | 0              | 0  | 0  | 0   | 0   | 0   | 0   | 0   |
| Access | read and write |    |    |     |     |     |     |     |

Table 56: Description of voice ADC input amplifier gain register bits

| Bit     | Symbol  | Description   |
|---------|---------|---|
| 15 to 8 | -       | not used  |
| 7 to 5  | -       | default 000   |
| 4 to 0  | IV[4:0] | <b>Voice ADC input amplifier gain.</b> A 5-bit value to program the voice amplifier gain in steps of 1.5 dB (21 settings). Default 0 0000. See <a href="#">Table 57</a> . |

Table 57: Voice ADC input amplifier gain bits

| IV4 | IV3 | IV2 | IV1 | IV0 | Gain (dB)   |
|-----|-----|-----|-----|-----|-------------|
| 0   | 0   | 0   | 0   | 0   | 0 (default) |
| 0   | 0   | 0   | 0   | 1   | +1.5        |
| 0   | 0   | 0   | 1   | 0   | +3          |
| 0   | 0   | 0   | 1   | 1   | +4.5        |
| 0   | 0   | 1   | 0   | 0   | +6          |
| 0   | 0   | 1   | 0   | 1   | +7.5        |
| :   | :   | :   | :   | :   | :           |
| 1   | 0   | 0   | 1   | 1   | +28.5       |
| 1   | 0   | 1   | 0   | 0   | +30         |
| :   | :   | :   | :   | :   | not used    |
| 1   | 1   | 1   | 1   | 1   | not used    |

### 11.13 Supplemental settings 1

Table 58: Supplemental settings 1 register (address 30h) bit allocation

| Bit    | 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|--------|----------------|----|----|----|----|----|---|---|
| Symbol | -              | -  | -  | -  | -  | -  | - | - |
| Reset  | 0              | 0  | 0  | 0  | 0  | 0  | 0 | 0 |
| Access | read and write |    |    |    |    |    |   |   |
| Bit    | 7              | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| Symbol | PDT            | -  | -  | -  | -  | -  | - | - |
| Reset  | 0              | 0  | 0  | 0  | 0  | 0  | 0 | 0 |
| Access | read and write |    |    |    |    |    |   |   |

Table 59: Description of supplemental settings 1 register bits

| Bit     | Symbol | Description  |
|---------|--------|--|
| 15 to 8 | -      | default 0000 0000  |
| 7       | PDT    | <b>Power down time.</b> Bit PDT selects the time of the SDAC power-down sequence.<br>1 = $1024/f_s$ seconds<br>0 = $512/f_s$ seconds (default) |
| 6 to 0  | -      | default 000 0000   |

### 11.14 Supplemental settings 2

Table 60: Supplemental settings 2 register (address 31h) bit allocation

| Bit    | 15             | 14    | 13    | 12    | 11 | 10 | 9    | 8     |
|--------|----------------|-------|-------|-------|----|----|------|-------|
| Symbol | -              | -     | -     | -     | -  | -  | -    | -     |
| Reset  | 0              | 0     | 0     | 0     | 0  | 0  | 0    | 0     |
| Access | read and write |       |       |       |    |    |      |       |
| Bit    | 7              | 6     | 5     | 4     | 3  | 2  | 1    | 0     |
| Symbol | -              | DITH2 | DITH1 | DITH0 | -  | -  | VMTP | PDLNA |
| Reset  | 0              | 0     | 0     | 0     | 0  | 0  | 0    | 0     |
| Access | read and write |       |       |       |    |    |      |       |

Table 61: Description of supplemental settings 2 register bits

| Bit     | Symbol    | Description  |
|---------|-----------|--|
| 15 to 7 | -         | default 0000 0000 0  |
| 6 to 4  | DITH[2:0] | <b>DAC dither control.</b> A 3-bit value to control the dithering of the SDAC. Default 000. See <a href="#">Table 62</a> .   |
| 3 to 2  | -         | default 00   |
| 1       | VMTP      | <b>Voice mute period control.</b> Bit VMPT selects the voice ADC mute period at power-up.<br>1 = mute for 1024 samples ( $1024/f_s$ )<br>0 = mute for 2048 samples ( $2048/f_s$ ; default) |

**Table 61: Description of supplemental settings 2 register bits ...continued**

| Bit | Symbol | Description   |
|-----|--------|---|
| 0   | PDLNA  | <b>Power-down voice LNA.</b> Bit PDLNA is to power-down the voice ADC LNA. It should be noted that disabling the LNA requires a recovery time defined by the external RC circuit.<br><br>1 = power-down<br>0 = power-on (default) |

**Table 62: DAC dither control bits**

| DITH2 | DITH1 | DITH0 | Function                       |
|-------|-------|-------|--------------------------------|
| 0     | 0     | 0     | DC dither (mid level); default |
| 0     | 0     | 1     | reserved                       |
| 0     | 1     | 0     | reserved                       |
| 0     | 1     | 1     | reserved                       |
| 1     | 0     | 0     | DC dither (low level)          |
| 1     | 0     | 1     | DC plus AC dither (low level)  |
| 1     | 1     | 0     | DC dither (high level)         |
| 1     | 1     | 1     | DC plus AC dither (high level) |

## 12. Limiting values

**Table 63: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                 | Parameter                       | Conditions | Min       | Max   | Unit |
|------------------------|---------------------------------|------------|-----------|-------|------|
| V <sub>DD</sub>        | supply voltage                  |            | [1] -     | 4.0   | V    |
| T <sub>xtal(max)</sub> | maximum crystal temperature     |            | -         | 150   | °C   |
| T <sub>stg</sub>       | storage temperature             |            | -65       | +125  | °C   |
| T <sub>amb</sub>       | ambient temperature             |            | -20       | +85   | °C   |
| V <sub>esd</sub>       | electrostatic discharge voltage | HBM        | [2] -2000 | +2000 | V    |
|                        |                                 | MM         | [2] -200  | +200  | V    |

[1] All supply connections must be made to the same power supply.

[2] ESD behavior is tested in accordance with JEDEC II standard:

- a) Human Body Model (HBM); equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
- b) Machine Model (MM); equivalent to discharging a 200 pF capacitor through a 0.75 μH series inductor.

## 13. Thermal characteristics

**Table 64: Thermal characteristics**

| Symbol               | Parameter                                   | Conditions  | Typ | Unit |
|----------------------|---|-------------|-----|------|
| R <sub>th(j-a)</sub> | thermal resistance from junction to ambient | in free air | 85  | K/W  |



## 14. Static characteristics

**Table 65: Characteristics**

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $R_L = 22\text{ k}\Omega$ ; all voltages referenced to ground (pins  $V_{SS}$ ); unless otherwise specified.

| Symbol  | Parameter                                 | Conditions   | Min               | Typ              | Max               | Unit          |
|---|---|--|-------------------|------------------|-------------------|---------------|
| <b>Supplies</b>   |   |  |                   |                  |                   |               |
| $V_{DDA(AD)}$   | ADC analog supply voltage                 |  | [1] 2.7           | 3.3              | 3.6               | V             |
| $V_{DDA(DA)}$   | DAC analog supply voltage                 |  | [1] 2.7           | 3.3              | 3.6               | V             |
| $V_{DDD}$   | digital supply voltage                    |  | [1] 2.7           | 3.3              | 3.6               | V             |
| $I_{DDA(AD)}$   | ADC analog supply current                 | $f_{ADC} = 48\text{ kHz}$  | -                 | 30               | -                 | mA            |
|   |   | $f_{ADC} = 96\text{ kHz}$  | -                 | 31               | -                 | mA            |
| $I_{DDA(DA)}$   | DAC analog supply current                 | $f_{DAC} = 48\text{ kHz}$  | -                 | 20               | -                 | mA            |
|   |   | $f_{DAC} = 96\text{ kHz}$  | -                 | 32               | -                 | mA            |
| $I_{DDD}$   | digital supply current                    | $f_{ADC} = f_{DAC} = 48\text{ kHz}$ ;<br>$f_{VOICE} = 48\text{ kHz}$ | -                 | 31               | -                 | mA            |
|   |   | $f_{ADC} = f_{DAC} = 96\text{ kHz}$ ;<br>$f_{VOICE} = 48\text{ kHz}$ | -                 | 55               | -                 | mA            |
| $I_{DDD(pd)}$   | digital supply current in Power down-mode | audio and voice ADCs power-down                                      | -                 | 18               | -                 | mA            |
|   |   | DAC power-down   | -                 | 14               | -                 | mA            |
| <b>Digital input pins (5 V tolerant TTL compatible)</b> |   |  |                   |                  |                   |               |
| $V_{IH}$  | HIGH-level input voltage                  |  | 2.0               | -                | -                 | V             |
| $V_{IL}$  | LOW-level input voltage                   |  | -                 | -                | 0.8               | V             |
| $ I_{LI} $  | input leakage current                     |  | -                 | -                | 1                 | $\mu\text{A}$ |
| $C_i$   | input capacitance                         |  | -                 | -                | 10                | pF            |
| <b>Digital output pins</b>                              |   |  |                   |                  |                   |               |
| $V_{OH}$  | HIGH-level output voltage                 | $I_{OH} = -2\text{ mA}$  | $0.85V_{DDD}$     | -                | -                 | V             |
| $V_{OL}$  | LOW-level output voltage                  | $I_{OL} = 2\text{ mA}$   | -                 | -                | 0.4               | V             |
| <b>Analog-to-digital converter</b>                      |   |  |                   |                  |                   |               |
| $V_{ref}$   | reference voltage on pin $V_{ref}$        | with respect to $V_{SSA(AD)}$  | $0.45V_{DDA(AD)}$ | $0.5V_{DDA(AD)}$ | $0.55V_{DDA(AD)}$ | V             |
| $V_{ADCP}$  | positive reference voltage of ADC         |  | -                 | $V_{DDA(AD)}$    | -                 | V             |
| $V_{ADCN}$  | negative reference voltage of ADC         |  | 0.0               | 0.0              | 0.0               | V             |
| $R_o$   | output resistance on pin $V_{ref}$        |  | -                 | 5                | -                 | k $\Omega$    |
| $R_{i(ADC)}$  | input resistance of audio ADC             |  | -                 | 10               | -                 | k $\Omega$    |

**Table 65: Characteristics ...continued**

$V_{DD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $R_L = 22\text{ k}\Omega$ ; all voltages referenced to ground (pins  $V_{SS}$ ); unless otherwise specified.

| Symbol                             | Parameter                     | Conditions | Min | Typ | Max | Unit             |
|------------------------------------|-------------------------------|------------|-----|-----|-----|------------------|
| $R_{i(VADC)}$                      | input resistance of voice ADC |            | -   | 5   | -   | $\text{k}\Omega$ |
| <b>Digital-to-analog converter</b> |                               |            |     |     |     |                  |
| $R_L$                              | load resistance               |            | 4   | -   | -   | $\text{k}\Omega$ |
| $R_o$                              | output resistance             |            | -   | 1   | -   | $\text{k}\Omega$ |

[1] All supply connections must be made to the same power supply unit.

## 15. Dynamic characteristics

**Table 66: Characteristics**

$V_{DD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3\text{ V}$ ;  $f_i = 1\text{ kHz}$ ;  $T_{amb} = 25\text{ °C}$ ;  $R_L = 22\text{ k}\Omega$ ; sampling frequency  $f_s = 48\text{ kHz}$ ; all voltages referenced to ground (pins  $V_{SS}$ ); unless otherwise specified.

| Symbol                                   | Parameter                                | Conditions                     | Min    | Typ  | Max  | Unit |    |
|--|--|--------------------------------|--------|------|------|------|----|
| <b>Audio analog-to-digital converter</b> |  |                                |        |      |      |      |    |
| $D_0$                                    | digital output level                     | at 0 dB setting; 900 mV input  | [1][2] | -2.5 | -1.2 | -0.7 | dB |
|  |  | at 3 dB setting; 637 mV input  | [2]    | -    | -1.2 | -    | dB |
|  |  | at 6 dB setting; 451 mV input  | [2]    | -    | -1.2 | -    | dB |
|  |  | at 9 dB setting; 319 mV input  | [2]    | -    | -1.2 | -    | dB |
|  |  | at 12 dB setting; 226 mV input | [2]    | -    | -1.2 | -    | dB |
|  |  | at 15 dB setting; 160 mV input | [2]    | -    | -1.2 | -    | dB |
|  |  | at 18 dB setting; 113 mV input | [2]    | -    | -1.2 | -    | dB |
|  |  | at 21 dB setting; 80 mV input  | [2]    | -    | -1.2 | -    | dB |
|  |  | at 24 dB setting; 57 mV input  | [2]    | -    | -1.2 | -    | dB |
| $\Delta V_i$                             | input voltage unbalance between channels |                                | -      | 0.1  | -    | dB   |    |

**Table 66: Characteristics ...continued**

$V_{DD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3\text{ V}$ ;  $f_i = 1\text{ kHz}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $R_L = 22\text{ k}\Omega$ ; sampling frequency  $f_s = 48\text{ kHz}$ ; all voltages referenced to ground (pins  $V_{SS}$ ); unless otherwise specified.

| Symbol                                   | Parameter  | Conditions  | Min | Typ   | Max | Unit |  |
|--|--|---|-----|-------|-----|------|--|
| (THD + N)/S                              | total harmonic distortion-plus-noise to signal ratio | normal mode; at -1 dBFS                                   |     |       |     |      |  |
|  |  | at 0 dB setting   | -   | -88   | -82 | dB   |  |
|  |  | at 3 dB setting   | -   | -88   | -   | dB   |  |
|  |  | at 6 dB setting   | -   | -88   | -   | dB   |  |
|  |  | at 9 dB setting   | -   | -88   | -   | dB   |  |
|  |  | at 12 dB setting  | -   | -88   | -   | dB   |  |
|  |  | at 15 dB setting  | -   | -87   | -   | dB   |  |
|  |  | at 18 dB setting  | -   | -85   | -   | dB   |  |
|  |  | at 21 dB setting  | -   | -83   | -   | dB   |  |
|  |  | at 24 dB setting  | -   | -82   | -   | dB   |  |
|  |  | normal mode; at -60 dBFS;<br>A-weighted                   |     |       |     |      |  |
|  |  | at 0 dB setting   | -   | -37   | -30 | dB   |  |
|  |  | at 3 dB setting   | -   | -37   | -   | dB   |  |
|  |  | at 6 dB setting   | -   | -37   | -   | dB   |  |
|  |  | at 9 dB setting   | -   | -37   | -   | dB   |  |
|  |  | at 12 dB setting  | -   | -37   | -   | dB   |  |
|  |  | at 15 dB setting  | -   | -37   | -   | dB   |  |
|  |  | at 18 dB setting  | -   | -35   | -   | dB   |  |
| at 21 dB setting                         | -  | -32   | -   | dB    |     |      |  |
| at 24 dB setting                         | -  | -30   | -   | dB    |     |      |  |
| S/N                                      | signal-to-noise ratio                                | code = 0; A-weighted                                      | 89  | 98    | -   | dB   |  |
| $\alpha_{CS}$                            | channel separation                                   |   | -   | 100   | -   | dB   |  |
| <b>Voice analog-to-digital converter</b> |  |   |     |       |     |      |  |
| $V_{i(rms)}$                             | input voltage (RMS value)                            | at 0 dBFS digital output; 2.2 k $\Omega$ source impedance | -   | 50.0  | -   | mV   |  |
| (THD + N)/S                              | total harmonic distortion-plus-noise to signal ratio | at -1 dBFS  | -   | -78   | -   | dB   |  |
|  |  | at -20 dBFS   | -   | -65   | -   | dB   |  |
|  |  | at -40 dBFS; A-weighted                                   | -   | -47   | -   | dB   |  |
| S/N                                      | signal-to-noise ratio                                | code = 0; A-weighted                                      | -   | 87    | -   | dB   |  |
| <b>Digital-to-analog converter</b>       |  |   |     |       |     |      |  |
| <b>Differential mode</b>                 |  |   |     |       |     |      |  |
| $V_{o(rms)}$                             | output voltage (RMS value)                           | at 0 dBFS digital input                                   | 1.9 | 2.0   | 2.1 | V    |  |
| $\Delta V_o$                             | output voltage unbalance between channels            |   | -   | < 0.1 | -   | dB   |  |
| (THD + N)/S                              | total harmonic distortion-plus-noise to signal ratio | at 0 dBFS   | -   | -98   | -93 | dB   |  |
|  |  | at -20 dBFS   | -   | -90   | -   | dB   |  |
|  |  | at -60 dBFS; A-weighted                                   | -   | -50   | -45 | dB   |  |
| S/N                                      | signal-to-noise ratio                                | code = 0; A-weighted                                      | 100 | 110   | -   | dB   |  |
| $\alpha_{CS}$                            | channel separation                                   |   | -   | 114   | -   | dB   |  |

**Table 66: Characteristics ...continued**

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3\text{ V}$ ;  $f_i = 1\text{ kHz}$ ;  $T_{amb} = 25\text{ °C}$ ;  $R_L = 22\text{ k}\Omega$ ; sampling frequency  $f_s = 48\text{ kHz}$ ; all voltages referenced to ground (pins  $V_{SS}$ ); unless otherwise specified.

| Symbol                   | Parameter  | Conditions              | Min | Typ   | Max | Unit |
|--------------------------|--|-------------------------|-----|-------|-----|------|
| <b>Single-ended mode</b> |  |                         |     |       |     |      |
| $V_{O(rms)}$             | output voltage (RMS value)                           | at 0 dBFS digital input | -   | 1.0   | -   | V    |
| $\Delta V_o$             | output voltage unbalance between channels            |                         | -   | < 0.1 | -   | dB   |
| (THD + N)/S              | total harmonic distortion-plus-noise to signal ratio | at 0 dBFS               | -   | -88   | -   | dB   |
|                          |  | at -20 dBFS             | -   | -85   | -   | dB   |
|                          |  | at -60 dBFS; A-weighted | -   | -45   | -   | dB   |
| S/N                      | signal-to-noise ratio                                | code = 0; A-weighted    | -   | 105   | -   | dB   |
| $\alpha_{cs}$            | channel separation                                   |                         | -   | 110   | -   | dB   |

[1] The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.

[2] The input voltage to the ADC scales proportionally with the power supply voltage.

## 15.1 Timing

**Table 67: Timing**

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = 2.7\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -20\text{ °C to }+85\text{ °C}$ ; typical timing specified at sampling frequency  $f_s = 48\text{ kHz}$ ; unless otherwise specified.

| Symbol                              | Parameter               | Conditions                     | Min          | Typ | Max          | Unit |
|-------------------------------------|-------------------------|--------------------------------|--------------|-----|--------------|------|
| <b>System clock (see Figure 16)</b> |                         |                                |              |     |              |      |
| $T_{sys}$                           | system clock cycle time | $f_{sys} = 256f_s$             | [1] 35       | 81  | 780          | ns   |
|                                     |                         | $f_{sys} = 384f_s$             | [1] 23       | 54  | 520          | ns   |
|                                     |                         | $f_{sys} = 512f_s$             | [1] 17       | 41  | 390          | ns   |
|                                     |                         | $f_{sys} = 768f_s$             | [1] 17       | 27  | 260          | ns   |
| $t_{CWL}$                           | system clock LOW time   | $f_{sys} < 19.2\text{ MHz}$    | $0.3T_{sys}$ | -   | $0.7T_{sys}$ | ns   |
|                                     |                         | $f_{sys} \geq 19.2\text{ MHz}$ | $0.4T_{sys}$ | -   | $0.6T_{sys}$ | ns   |
| $t_{CWH}$                           | system clock HIGH time  | $f_{sys} < 19.2\text{ MHz}$    | $0.3T_{sys}$ | -   | $0.7T_{sys}$ | ns   |
|                                     |                         | $f_{sys} \geq 19.2\text{ MHz}$ | $0.4T_{sys}$ | -   | $0.6T_{sys}$ | ns   |

### I<sup>2</sup>S-bus interface

Serial data of audio ADC and DAC (see Figure 17)

|                 |                           |       |    |   |      |     |
|-----------------|---------------------------|-------|----|---|------|-----|
| $f_{BCK}$       | audio bit clock frequency | [2] - | -  | - | 12.8 | MHz |
| $T_{cy(BCK)}$   | BCK cycle time            | -     | -  | - | 78   | ns  |
| $t_{BCKH}$      | bit clock HIGH time       | -     | 30 | - | -    | ns  |
| $t_{BCKL}$      | bit clock LOW time        | -     | 30 | - | -    | ns  |
| $t_r$           | rise time                 | -     | -  | - | 20   | ns  |
| $t_f$           | fall time                 | -     | -  | - | 20   | ns  |
| $t_{su(WS)}$    | word select set-up time   | -     | 10 | - | -    | ns  |
| $t_h(WS)$       | word select hold time     | -     | 10 | - | -    | ns  |
| $t_{su(DATAI)}$ | data input set-up time    | -     | 10 | - | -    | ns  |
| $t_h(DATAI)$    | data input hold time      | -     | 10 | - | -    | ns  |
| $t_h(DATAO)$    | data output hold time     | -     | 0  | - | -    | ns  |

**Table 67: Timing ...continued**

$V_{DDD} = V_{DDA(AD)} = V_{DDA(AD)} = 2.7\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -20\text{ °C to }+85\text{ °C}$ ; typical timing specified at sampling frequency  $f_s = 48\text{ kHz}$ ; unless otherwise specified.

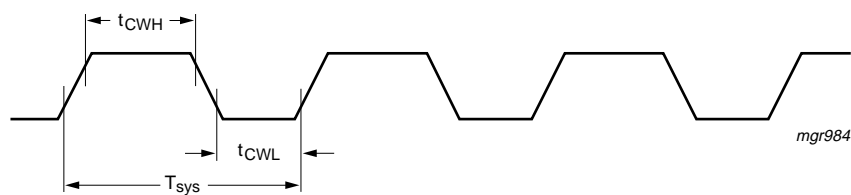
| Symbol  | Parameter  | Conditions   | Min   | Typ | Max  | Unit |
|---|--|--------------|-------|-----|------|------|
| $t_{d(DATAO-BCKV)}$                                   | data output to bit clock delay                       |              | -     | -   | 30   | ns   |
| $t_{d(DATAO-WS)}$                                     | data output to word select delay                     |              | -     | -   | 30   | ns   |
| <b>Serial data of voice ADC</b>                       |  |              |       |     |      |      |
| $f_{BCKV}$  | voice bit clock frequency                            |              | [2] - | -   | 6.4  | MHz  |
| $T_{cy(BCKV)}$  | BCKV cycle time                                      |              | -     | -   | 156  | ns   |
| $t_{BCKVH}$   | bit clock HIGH time                                  |              | 50    | -   | -    | ns   |
| $t_{BCKVL}$   | bit clock LOW time                                   |              | 50    | -   | -    | ns   |
| $t_r$   | rise time  |              | -     | -   | 20   | ns   |
| $t_f$   | fall time  |              | -     | -   | 20   | ns   |
| $t_{su(WSV)}$   | word select set-up time                              |              | 10    | -   | -    | ns   |
| $t_h(WSV)$  | word select hold time                                |              | 10    | -   | -    | ns   |
| $t_h(DATAV)$  | data output hold time                                |              | 0     | -   | -    | ns   |
| $t_{d(DATAV-BCKV)}$                                   | data output to bit clock delay                       |              | -     | -   | 30   | ns   |
| $t_{d(DATAV-WSV)}$                                    | data output to word select delay                     |              | -     | -   | 30   | ns   |
| $t_{d(WSV-BCKV)}$                                     | word select to bit clock delay                       | WSV-out mode | -30   | -   | +30  | ns   |
| <b>L3-bus interface (see Figure 18 and Figure 19)</b> |  |              |       |     |      |      |
| <b>L3CLOCK timing</b>                                 |  |              |       |     |      |      |
| $f_{cy(CLK)L3}$                                       | L3CLOCK frequency                                    |              | -     | -   | 2000 | kHz  |
| $T_{cy(CLK)L3}$                                       | L3CLOCK cycle time                                   |              | 500   | -   | -    | ns   |
| $t_{CLK(L3)H}$  | L3CLOCK HIGH time                                    |              | 250   | -   | -    | ns   |
| $t_{CLK(L3)L}$  | L3CLOCK LOW time                                     |              | 250   | -   | -    | ns   |
| <b>L3MODE timing</b>                                  |  |              |       |     |      |      |
| $t_{su(L3)A}$   | L3MODE set-up time in address mode                   |              | 190   | -   | -    | ns   |
| $t_h(L3)A$  | L3MODE hold time in address mode                     |              | 190   | -   | -    | ns   |
| $t_{su(L3)D}$   | L3MODE set-up time in data transfer mode             |              | 190   | -   | -    | ns   |
| $t_h(L3)D$  | L3MODE hold time in data transfer mode               |              | 190   | -   | -    | ns   |
| $t_{stp(L3)}$   | L3MODE stop time in data transfer mode               |              | 190   | -   | -    | ns   |
| <b>L3DATA timing</b>                                  |  |              |       |     |      |      |
| $t_{su(L3)DA}$  | L3DATA set-up time in data transfer and address mode |              | 190   | -   | -    | ns   |
| $t_h(L3)DA$   | L3DATA hold time in data transfer and address mode   |              | 30    | -   | -    | ns   |
| $t_{d(L3)R}$  | L3DATA delay time for read data                      |              | 0     | -   | 50   | ns   |

**Table 67: Timing ...continued**

$V_{DD3} = V_{DDA(AD)} = V_{DDA(AD)} = 2.7\text{ V to }3.6\text{ V}$ ;  $T_{amb} = -20\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; typical timing specified at sampling frequency  $f_s = 48\text{ kHz}$ ; unless otherwise specified.

| Symbol   | Parameter                                      | Conditions | Min               | Typ | Max | Unit          |
|--|--|------------|-------------------|-----|-----|---------------|
| $t_{dis(L3)R}$   | L3DATA disable time for read data              |            | 0                 | -   | 50  | ns            |
| <b>I<sup>2</sup>C-bus interface timing (see Figure 20)</b> |  |            |                   |     |     |               |
| <b>SCL timing</b>  |  |            |                   |     |     |               |
| $f_{SCL}$  | SCL clock frequency                            |            | 0                 | -   | 400 | kHz           |
| $t_{LOW}$  | SCL LOW time                                   |            | 1.3               | -   | -   | $\mu\text{s}$ |
| $t_{HIGH}$   | SCL HIGH time                                  |            | 0.6               | -   | -   | $\mu\text{s}$ |
| $t_r$  | rise time SDA and SCL                          |            | [3] $20 + 0.1C_b$ | -   | 300 | ns            |
| $t_f$  | fall time SDA and SCL                          |            | [3] $20 + 0.1C_b$ | -   | 300 | ns            |
| <b>SDA timing</b>  |  |            |                   |     |     |               |
| $t_{BUF}$  | bus free time between STOP and START condition |            | 1.3               | -   | -   | $\mu\text{s}$ |
| $t_{SU,STA}$   | set-up time repeated START                     |            | 0.6               | -   | -   | $\mu\text{s}$ |
| $t_{HD,STA}$   | hold time START condition                      |            | 0.6               | -   | -   | $\mu\text{s}$ |
| $t_{SU,DAT}$   | data set-up time                               |            | 100               | -   | -   | ns            |
| $t_{HD,DAT}$   | data hold time                                 |            | 0                 | -   | -   | $\mu\text{s}$ |
| $t_{SU,STO}$   | set-up time STOP condition                     |            | 0.6               | -   | -   | $\mu\text{s}$ |
| $t_{SP}$   | pulse width of spikes                          |            | [4] 0             | -   | 50  | ns            |
| $C_b$  | capacitive load for each bus line              |            | -                 | -   | 400 | pF            |

- [1] The system clock should not exceed 58 MHz in any mode.
- [2] The bit clock frequency should not exceed 256 times the corresponding sampling frequency.
- [3]  $C_b$  is the total capacitance for each bus line.
- [4] To be suppressed by the input filter.



**Fig 16. System clock timing**

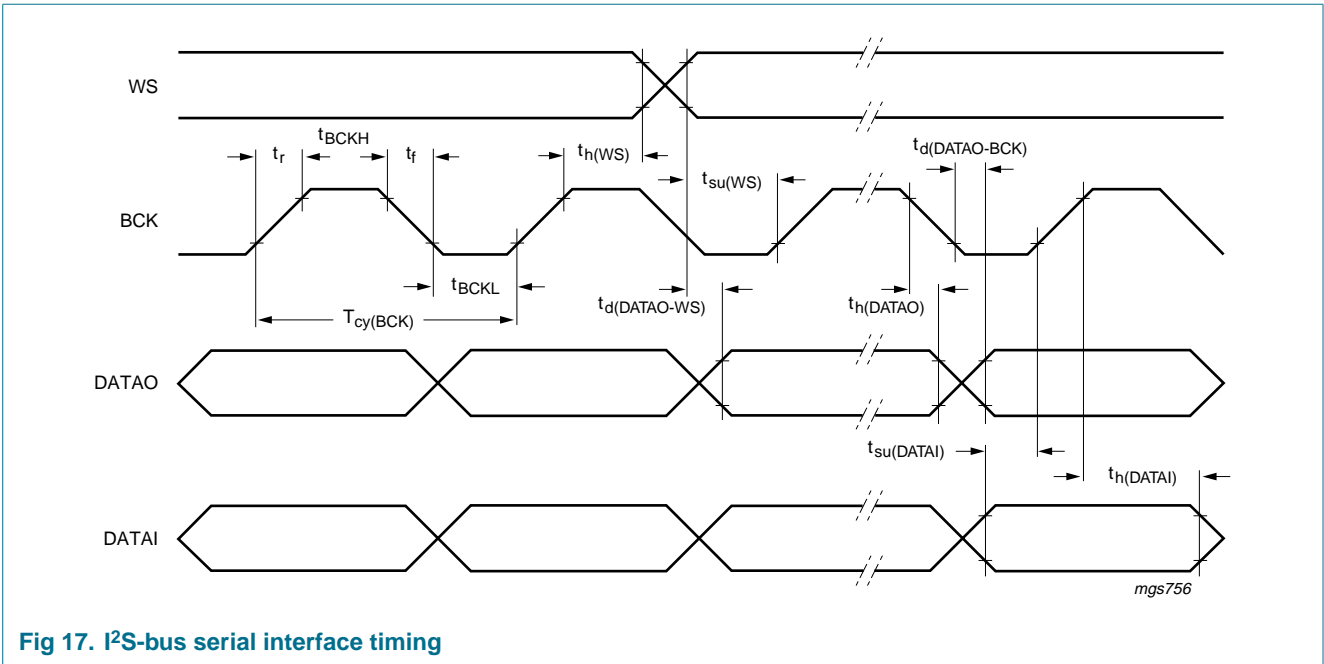


Fig 17. I<sup>2</sup>S-bus serial interface timing

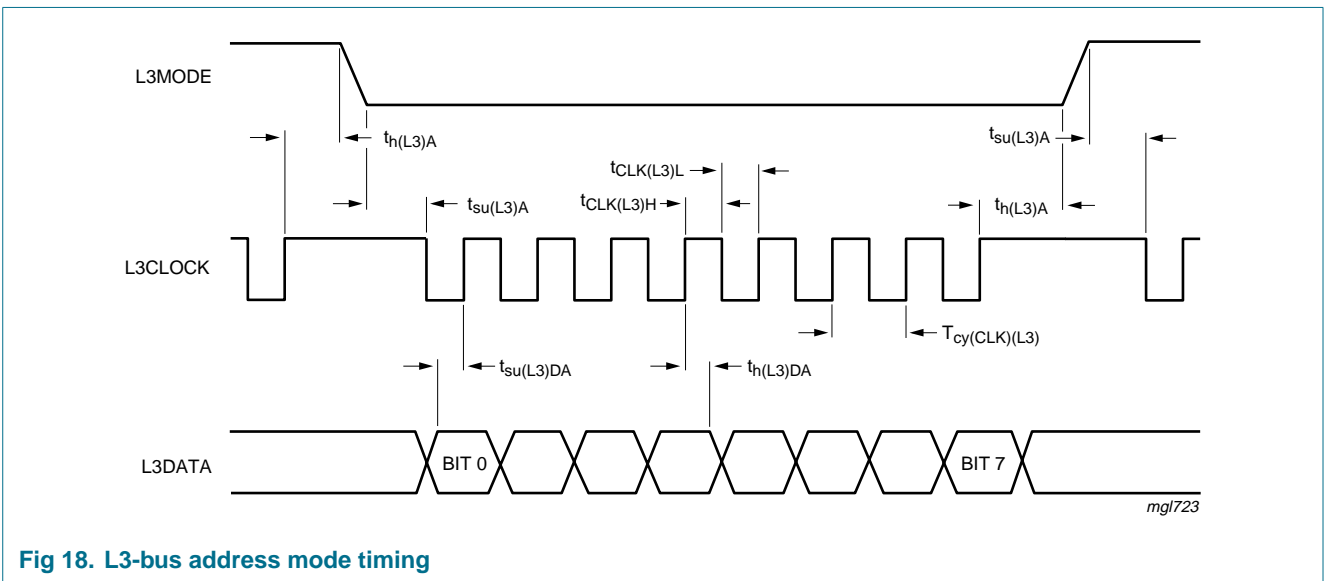
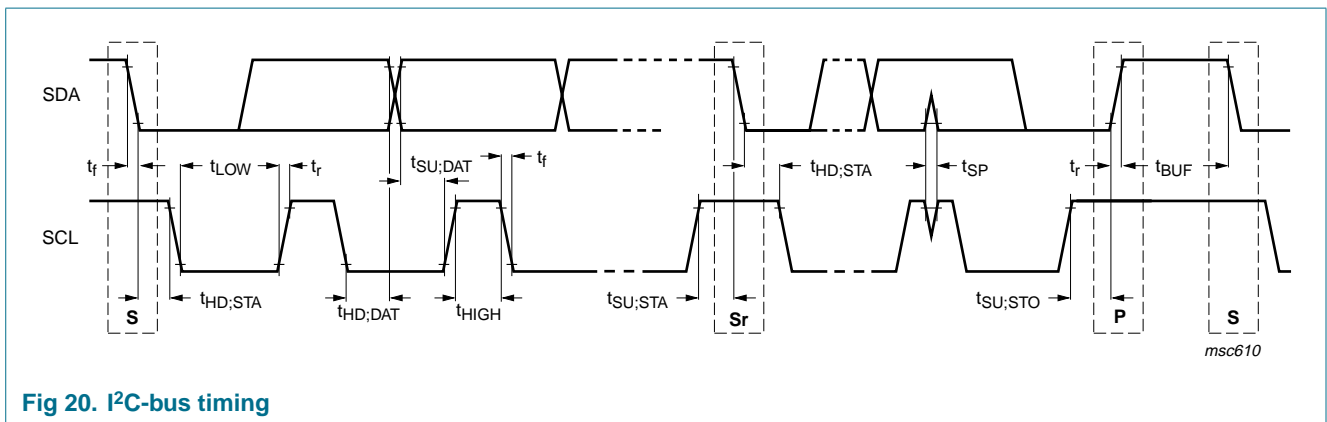
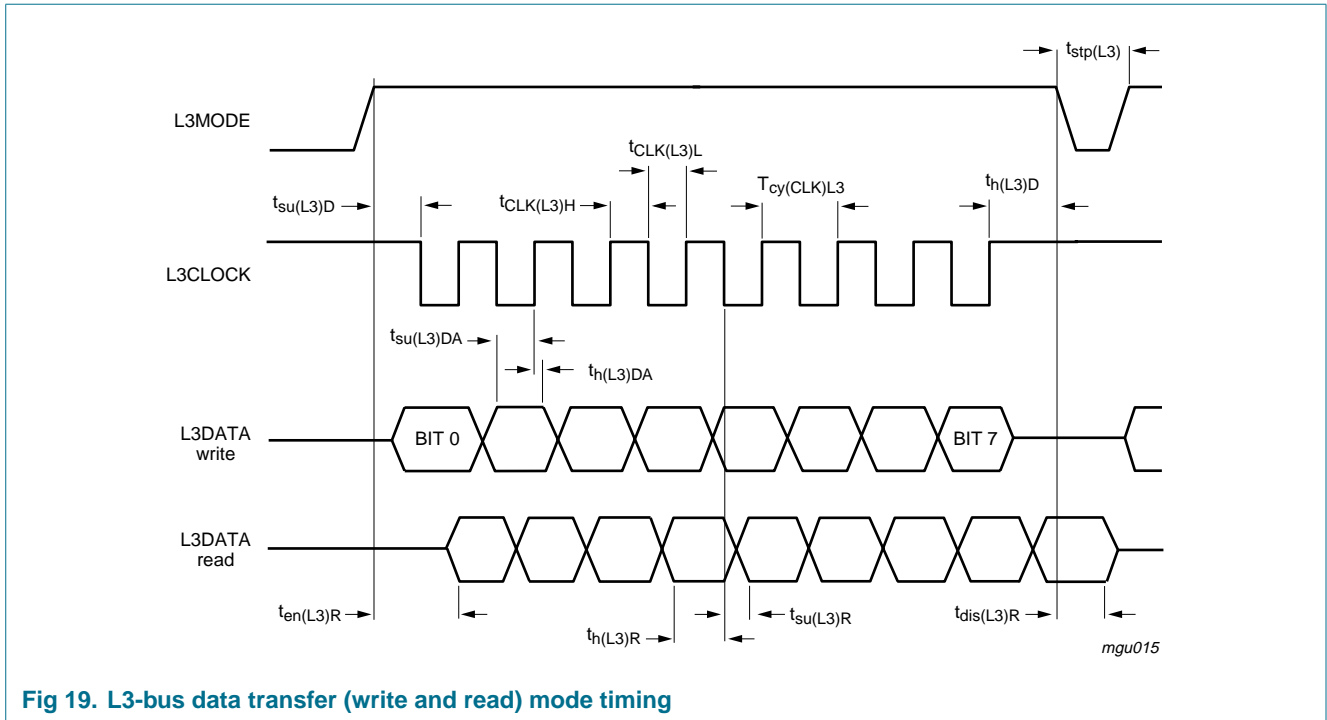


Fig 18. L3-bus address mode timing



## 16. Test information

### 16.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.



17. Package outline

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2

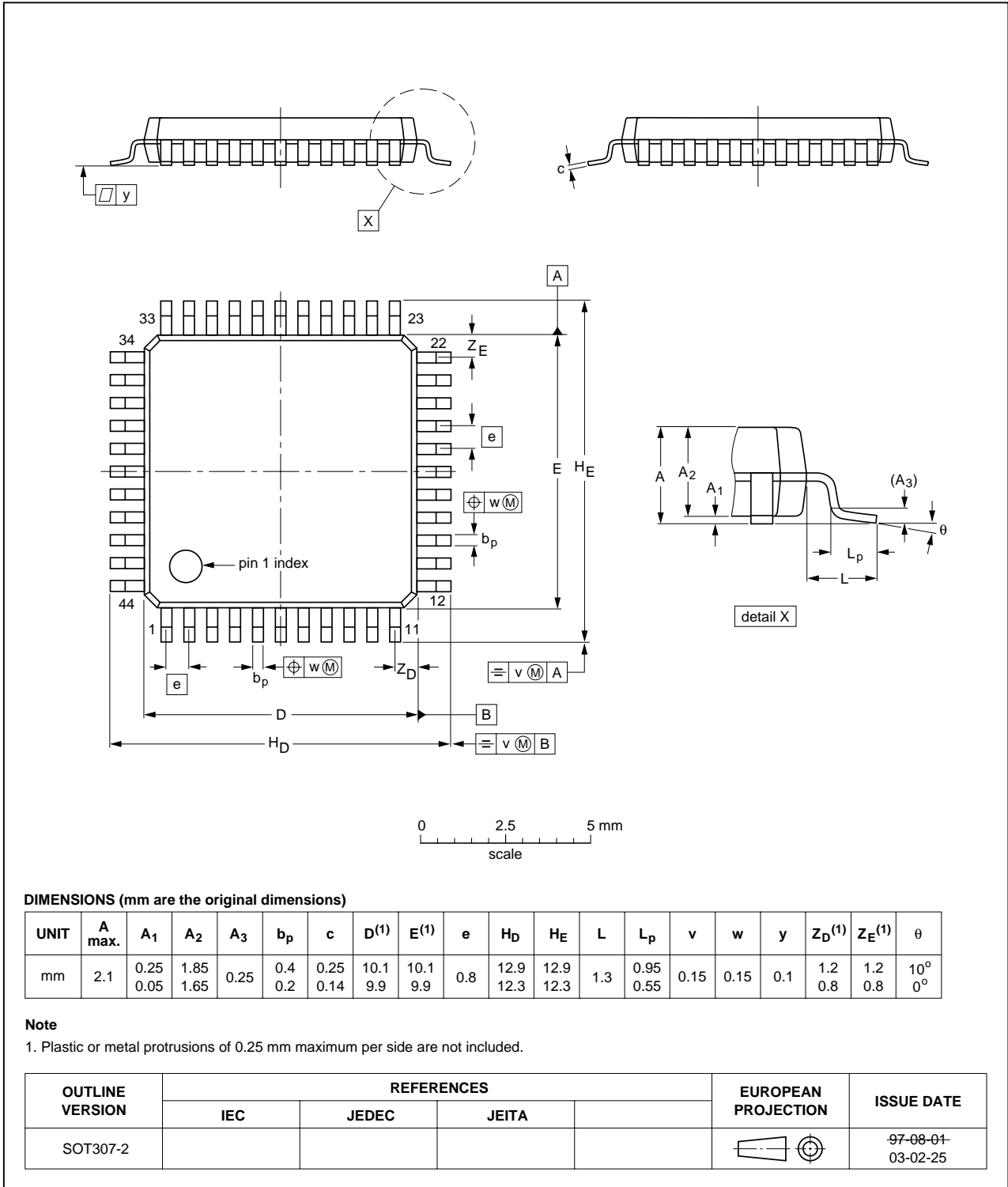


Fig 21. Package outline SOT307-2 (QFP44)

## 18. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## 19. Soldering

### 19.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 19.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### 19.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 19.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

### 19.5 Package related soldering information

**Table 68: Suitability of surface mount IC packages for wave and reflow soldering methods**

| Package <sup>[1]</sup>   | Soldering method                   |                       |
|--|------------------------------------|-----------------------|
|  | Wave                               | Reflow <sup>[2]</sup> |
| BGA, HTSSON..T <sup>[3]</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>[3]</sup> , TFBGA, VFBGA, XSON | not suitable                       | suitable              |
| DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS           | not suitable <sup>[4]</sup>        | suitable              |
| PLCC <sup>[5]</sup> , SO, SOJ  | suitable                           | suitable              |
| LQFP, QFP, TQFP  | not recommended <sup>[5] [6]</sup> | suitable              |
| SSOP, TSSOP, VSO, VSSOP  | not recommended <sup>[7]</sup>     | suitable              |
| CWQCCN..L <sup>[8]</sup> , PMFP <sup>[9]</sup> , WQCCN..L <sup>[8]</sup>                       | not suitable                       | not suitable          |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note (AN01026)*; order a copy from your Philips Semiconductors sales office.

- [2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.
- [3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217\text{ °C} \pm 10\text{ °C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a  $45^\circ$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

## 20. Revision history

Table 69: Revision history

| Document ID    | Release date   | Data sheet status         | Change notice | Doc. number    | Supersedes |
|----------------|--|---------------------------|---------------|----------------|------------|
| UDA1384_2      | 20050117   | Product data sheet        | -             | 9397 750 14366 | UDA1384_1  |
| Modifications: | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors</li> <li><a href="#">Section 4 "Quick reference data"</a>: Added values for <math>I_{DDD(pd)}</math></li> <li><a href="#">Section 14 "Static characteristics"</a>: Added values for <math>I_{DDD(pd)}</math></li> <li><a href="#">Section 15 "Dynamic characteristics"</a>: Removed PSRR specification and (THD+N)/S at -20 dBFS, added (THD+N)/S for DAC differential mode</li> </ul> |                           |               |                |            |
| UDA1384_1      | 20031009   | Preliminary specification | -             | 9397 750 12043 | -          |

## 21. Data sheet status

| Level | Data sheet status <sup>[1]</sup> | Product status <sup>[2]</sup> <sup>[3]</sup> | Definition   |
|-------|----------------------------------|--|--|
| I     | Objective data                   | Development                                  | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
| II    | Preliminary data                 | Qualification                                | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.             |
| III   | Product data                     | Production                                   | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 22. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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